

# Worst Case Circuit Analysis

## Have We Forgotten What Works?

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presented by:  
Charles Hymowitz of AEI Systems

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“Satellite designers have crossed a threshold. We are fielding on-board compute that rivals terrestrial edge servers... The hard limit on mission capability is not the processor data sheet — it is whether the power architecture can deliver sub-volt rails at hundreds of amperes, with microsecond-class transient performance.”

Nearly 100% of the designs we analyze fail power integrity



ANALYTICAL HEAVY LIFTING

“Why Power Architectures Constrain New Space AI Missions”, Ken Coffman Vicor, April 2026

Worst Case Circuit Analysis remains essential because modern space systems are becoming more complex at the same time budgets, schedules, and engineering resources are being compressed. As programs rely more heavily on reference designs, COTS parts, and test-based validation/verification, they are at risk of losing the analytical discipline that historically protected mission reliability.


The central question is whether we have forgotten the value of proven methods such as WCCA and Stress & Derating analysis. These methods help identify day-one risks, end-of-life risks, and design sensitivities before they become mission failures. The challenge is especially acute in power architectures, where advanced onboard processing is driving sub 3.3V rails, very high dynamic currents, and fast transient demands.

Testing alone is not enough to understand these systems because many critical margins and corner cases are difficult or impossible to reproduce in the limited hardware testing that is performed.


The presentation argues for targeted, intelligent analysis that complements test and restores rigor where it matters most. The goal is not to analyze everything blindly, but to make sure the right analyses are performed early enough to influence design decisions.

## The Core of What AEi Systems Does


- **WCCA, Reliability SDRLs**
  - ❖ Our 30th Year
  - ❖ Space, Aero, Automotive
    - **Modeling Support**



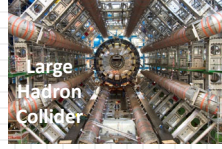
**Reliability Analysis**



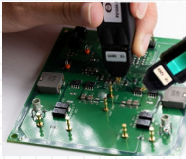
Europa Clipper




HALO



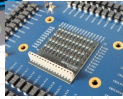
Large Hadron Collider



Power Integrity Test

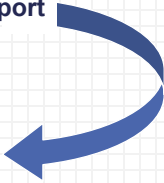


**PICOTEST**



ASIC/FPGA Load Stepper  
2000 Amps/ns

Image Credits: LMCO, BNL, NASA



AEi Systems is positioned at the intersection of reliability analysis, power system modeling, and power integrity testing. AEi has supported space, aerospace, and automotive programs for decades, with a core focus on WCCA, reliability deliverables, and circuit modeling. Picotest, founded by Steve Sandler after AEi, provides test products and measurement support for power supplies and power integrity applications. Together, AEi and Picotest see both sides of the problem: the analytical weaknesses found during WCCA and the practical limitations of power integrity testing. That combination gives AEi a broad view across many customers, programs, and design approaches. The work spans high-reliability systems ranging from spacecraft and accelerators to ASIC and FPGA power delivery.

This perspective is important because satellite reliability increasingly depends on power supply behavior, power distribution networks, and the interaction between test and analysis. AEi's experience shows that many of the same reliability issues repeat across programs when analysis is minimized or misunderstood.

## How are we doing on Mission Reliability?

### ■ Better, but data is fragmented – Few want to report

- ❖ Power Subsystem (EPS) failures are the most challenging to discern from anomaly data
- ❖ 13% of US military and 25% of commercial did not meet Design Life. EPS failures still one of top causes \*
- ❖ COTS parts increase EOL uncertainty and emerging technologies increase electrical risks
- ❖ Longer design life = more analysis = higher reliability

### ■ Takeaways:

- ❖ **EPS issues disproportionately impact mission life**
- ❖ **Design weakness—not parts—is a dominant limiter**  
Weak or overly sensitive designs are a more common reliability limiter than latent part defects, and neither part upscreening nor “high-reliability parts” can compensate for inadequate margins, insufficient circuit-level understanding, or unresolved design corner cases.

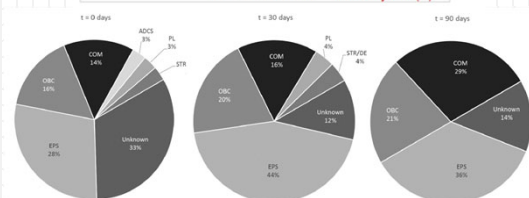
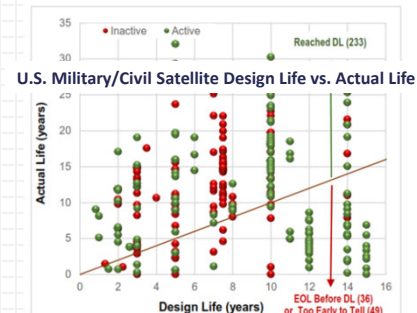


Figure 5: Subsystem contributions to CubeSat failure after ejection (incl. DOA), 30 days and 90 days  
\* NASA GSFC, Spacecraft Anomalies and Failures Workshop (SCAF), 2023

Mission reliability has improved in some areas, but the data is fragmented and difficult to interpret because many programs do not publicly report failures or anomalies. Electrical power subsystem failures are especially hard to identify from anomaly data, yet they remain a significant contributor to reduced mission life. The key point is that reliability is often limited less by defective parts and more by weak designs, sensitive circuits, and unresolved corner cases. Higher-grade parts and additional screening cannot compensate for inadequate margins or incomplete circuit understanding.

As spacecraft become more complex and COTS usage increases, end-of-life uncertainty and electrical risk increase as well. Longer design lives generally require more analysis, because more aging, radiation, tolerance, and environmental effects must be understood. The takeaway is that power systems are central to mission success, and small reductions in power system margin can have large mission consequences. WCCA helps reveal these vulnerabilities before they appear as on-orbit performance problems.

### References:

- 1) NASA GSFC, *Spacecraft Anomalies and Failures Workshop (SCAF)*, 2023–2024
- 2) Minow, J., *SCAF 2023 Introduction – Failure Trends* (NASA GSFC)
- 3) LExSO/GSFC, *Spacecraft Longevity and Reliability*, 2023
- 4) NASA GSFC, *Lessons Learned from On-Orbit Failures*, 2023
- 5) Aerospace Corp., *Space Power Workshop (SPW)*, 2023–2024
- 6) *Aerospace Journal*, LEO/GEO anomaly & radiation study, 2024

## What Are We Building?

- We have gone from multi-winding flybacks to OTS Converters and Multi-level Power Distribution Networks**
  - Dozens of Rails
  - We generally don't assess the converters (commodity, always stable, noiseless)
- Testing only at the top level, if that**
  - Engineering Unit? with Flight Parts?
- Takeaways:**
  - Noise permeates these systems and its operating mode dependent
  - Power rails are not one size fits all. They are each load dependent

Image Credit: IEEE EPEPS

ae systems  
ANALYTICAL HEAVY LIFTING

4

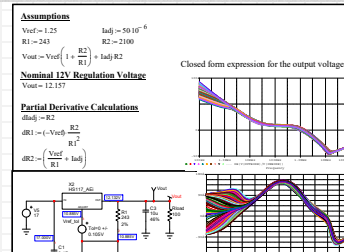
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“Why Power Architectures Constrain New Space AI Missions”, Ken Coffman Vicor, April 2026 - *“Satellite designers have crossed a threshold. We are no longer putting “a bit more DSP” in orbit; we are fielding on-board compute that rivals terrestrial edge servers, running AI inference, adaptive beamforming, dynamic spectrum management and real-time analytics at hundreds of TOPS. At that point, the hard limit on mission capability is not the processor data sheet — it is whether the power architecture can deliver sub-volt rails at hundreds of amperes, with microsecond-class transient performance, inside a small, thermally constrained, radiation-exposed enclosure.”*

Space power systems have shifted from simpler multi-winding flyback architectures to distributed power networks with off-the-shelf converters and many point-of-load rails. These systems are more flexible, but they also introduce more opportunities for noise, impedance resonances, load interactions, and mode-dependent behavior. Too often, converters are treated as commodity parts that are assumed to be stable, quiet, and interchangeable, even when the load and board environment say otherwise. Many programs test only at the top level, and sometimes not with representative flight hardware or realistic dynamic loading. Each power rail must be understood in the context of its actual load, decoupling, layout, and transient current demand. The move toward onboard AI, adaptive processing, and high-current sub-volt rails will make these problems harder, not easier. Future space systems will need power architectures that support fast transient response inside tight thermal, radiation, and volume constraints. That means power integrity and WCCA must be treated as design requirements, not afterthoughts.

## WCCA – What is it for?

- For many program managers - There is a distinct lack of understanding what WCCA is and does
  - ❖ NOT a check box (like MTBF)
- It is a process by which a design is vetted, nominally, as well as WC
  - ❖ Where do you think test limits come from?
- Functional Assessment (DC, AC, Transient), Part Calcs, Nominal & EOL Calc, Tolerance impacts, design assumptions – (Stress pairs not replaces!)
  - ❖ Like PCB DRC
- Analysis is key when test is limited – for instance when hardware is integrated
- WCCA is NOT just for EOL impacts
- It can be targeted but its often left out



Reasons to Perform Worst Case Analysis

Need	Reason
<b>Design Verification and Reliability</b>	Verifies circuit operation - quantify the risk/margins
	Determines sensitivities - To improve performance
	Verifies that a circuit interfaces
	Determines the impact of part failures
<b>Test Cost Reduction</b>	Evaluates performance aspects that can be measured
	Helps set ATP limits
	Reduces the amount and scope of testing
<b>Parts Assessment</b>	Determines part suitability
	Supports SCD requirements/screening
	To analyze Single Event Transients (SET)
	Supports transient Stress & Derating
<b>Schedule, Cost, or Contractual Risk Reduction</b>	Reduces board spins
	Verifies changes to heritage circuits
	To obtain better insurance rates or reduce contractual liabilities
	To avoid a catastrophic or costly incident
<b>Return on Investment</b>	Improves future products
	Improves knowledge and capability of your engineering staff

WCCA is often misunderstood as a contractual checkbox, but its real purpose is to vet whether a circuit will perform across nominal, beginning-of-life, and end-of-life conditions. It evaluates functional performance, sensitivities, tolerances, aging, radiation effects, transient behavior, and design assumptions.

WCCA also helps define realistic test limits because it shows where the circuit should operate and where the true margins are. The process is not limited to end-of-life calculations; it also identifies nominal design weaknesses and beginning-of-life risks. Stress & Derating analysis is important, but it does not replace WCCA because stress analysis answers a different question. WCCA is similar to a design rule check for circuit performance: it exposes where the design is sensitive, poorly margined, or dependent on assumptions that have not been verified. It is especially valuable when test access is limited or when hardware is already integrated. When properly targeted, WCCA reduces risk, focuses test dollars, and improves both the current design and future engineering capability.

# Where We Find Most Problems

All of these analyses typically have concerns

## Power Systems

- ❖ Regulation
- ❖ Filter Mismatches
- ❖ Startup/Inrush
- ❖ Control Loop Stability
- ❖ Power Integrity – Target Impedance and Q
- ❖ Power Sequencing
- ❖ Single Event Transient

## Derived Requirements (FET Gate Drive)

## Simple Circuits

## “Minor” Design Changes

## Reference Designs

## Interface Definition

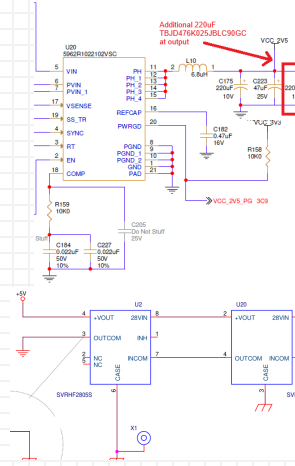
## Part Overstress – Especially Transient

## Signal Integrity Terminations Timing

## Data sheet violations, inadequate reference designs, bad vendor models

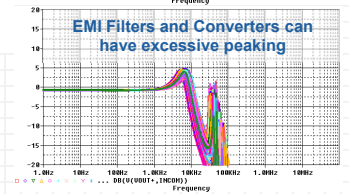
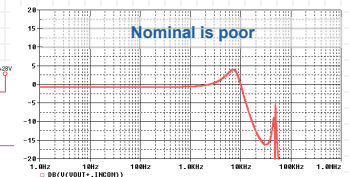
20-50% of the first pass WC analyses - don't pass!

“But It’s Just a Converter”



Parameter	Nominal	Parametric EVA	Monte Carlo EOL Results 99.93%/90%
Gain Margin	22.05dB	16.97dB - 46.99dB	25.09dB - 48.45dB
Phase Margin	48.30°	35.50° - 55.46°	22.72° - 72.53°

Stability can fall by 20-30 deg over life



AEi routinely finds problems in power systems, derived requirements, simple circuits, reference designs, minor design changes, interfaces, transient stress, and signal or power integrity. A surprising percentage of first-pass WCCA efforts on previously unanalyzed hardware reveal non-compliances. Many of these issues are not obvious in nominal testing because they occur only under tolerance, aging, temperature, transient, or interaction conditions. Power systems are especially vulnerable in areas such as regulation, startup, inrush, stability, filter mismatch, power sequencing, single-event transients, and PDN impedance. Derived requirements are another common gap because many circuits must perform correctly even when no explicit specification has been written for them. Simple circuits can be deceptively risky, especially high-Q filters, ferrite beads, references, optocouplers, relays, and unity-gain op amp configurations. Reference designs and vendor models are not a substitute for verification, because they may omit layout effects, load interactions, or worst-case assumptions. **The message is that these analyses are on the checklist because they repeatedly find real design risk.**

**Derived Requirements** - circuits that do not have specs but must work for the functional block to work

- Stability
- Current Limit, Inrush
- FET Gate Drive - BJT leakage and minimum hFE
- Opamps in unity gain configurations

### Simple Circuits

- High 'Q' Circuits, Filters, LC using ceramics, Beads
- Relays
- Opto-couplers
- Voltage and Zener References

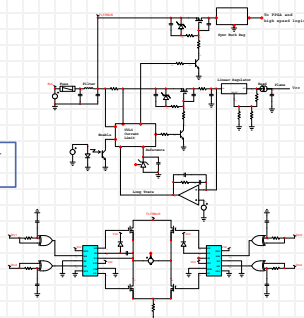
### Signal & Power Integrity

- SSO Noise, PDN Resonances → Regulation Outages
- Missing series termination resistors
- Monotonicity, Overshoot, Undershoot, improper terminations
- WC Timing
- EOL Logic Compatibility
- Power Sequencing

## Data Item Description Challenges

- Prime expectations for analysis are not sufficiently defined
 

"The WCCA analysis will verify the design functional margin based upon expected operating conditions for temperature design limits, individual piece-part tolerance, part aging, voltage and frequency tolerance."
- DIDs are generic
  - Do a good job – buyer doesn't know what functions are in the design, so they don't know what to tell subcontractor
  - TOR, LMCO, Boeing have checklists – but are often diminished
    - NASA, others have little to no SPECIFIC guidance
  - Buyers don't know what functional blocks are in the design and even then, generally don't guide
  - Manufacturer simply can not be left to define scope



### Point of Load Switching Regulator WCCA

Specifications, Requirements, Design Objectives

MODULE 1 – High Priority Analysis

- Stability
- Conducted Susceptibility
- Output Ripple
- Switching Frequency, Duty Cycle

Startup Times, Overshoot, Inrush, Shutdown

Load Step or PDN/AC Impedance (< 3.3V and/or Digital Load)

Voltage Regulation

Optional: Current Limit

MODULE 2 – Critical PBT Signals

- Cross-Conduction & Shoot-through
- MOSFET Current Shoot-Through: within SOA, avalanche, and operating
- Dead-Time: No cross-conduction
- MOSFET Current and Losses: Junction Temperature Rise
- Gate drive voltage threshold (on and off), lower and upper
- Gate drive current (on and off), lower and upper
- Gate drive waveforms rise / fall time in pre-driver
- Complex Load Stepping
- PWM dynamic range
- Peer Review

Item ID	Item Description	Analysis Method	Analysis Location	Analysis Status
1	Stability	AC Analysis	Power Stage	Complete
2	Conducted Susceptibility	EMC Analysis	Power Stage	In Progress
3	Output Ripple	Transient Analysis	Power Stage	Complete
4	Switching Frequency, Duty Cycle	Simulation	Power Stage	Complete
5	Startup Times, Overshoot, Inrush, Shutdown	Simulation	Power Stage	In Progress
6	Load Step or PDN/AC Impedance (< 3.3V and/or Digital Load)	Simulation	Power Stage	Complete
7	Voltage Regulation	Simulation	Power Stage	Complete
8	Optional: Current Limit	Simulation	Power Stage	Complete
9	Cross-Conduction & Shoot-through	Simulation	Power Stage	In Progress
10	MOSFET Current Shoot-Through: within SOA, avalanche, and operating	Simulation	Power Stage	In Progress
11	Dead-Time: No cross-conduction	Simulation	Power Stage	Complete
12	MOSFET Current and Losses: Junction Temperature Rise	Simulation	Power Stage	In Progress
13	Gate drive voltage threshold (on and off), lower and upper	Simulation	Power Stage	Complete
14	Gate drive current (on and off), lower and upper	Simulation	Power Stage	Complete
15	Gate drive waveforms rise / fall time in pre-driver	Simulation	Power Stage	Complete
16	Complex Load Stepping	Simulation	Power Stage	In Progress
17	PWM dynamic range	Simulation	Power Stage	Complete
18	Peer Review	Review	Power Stage	Complete

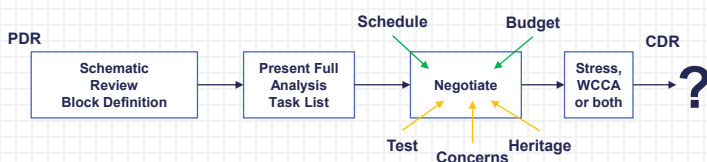
Many WCCA problems begin with vague or incomplete Customer Data Item Descriptions (DIDs) and insufficiently defined prime contractor expectations. Generic language such as “verify functional margin” does not tell the subcontractor which functional blocks, derived requirements, or high-risk behaviors must be analyzed and what specifically to analyze about them.

Buyers often do not know the full design content early enough to specify the necessary analysis scope, and subcontractors should not be left to define scope alone. Existing guidance and checklists can be useful, but they are often watered down, ignored, or applied inconsistently.

A better approach starts with the schematic and a functional-block checklist, then adds or removes analyses based on risk, mission class, test coverage, and design maturity. This creates an explicit analysis plan instead of a vague contractual deliverable. The goal is not to burden every program with the same analysis list, but to avoid missing the analyses that matter most. Clearer scope definition protects both the buyer and the supplier by aligning expectations before schedule and budget pressure make meaningful analysis difficult.

## How Programs End Up with Near Zero Analysis

- The common story that often playing out...  
**Customer fails to adequately bid, \$ Limits, Schedule, Spec/Design Churn, Fall back on outdated guidelines**



For Class B the most susceptible circuits to part parameter variations are analyzed. For Class C and D there may be little margin required and test may be used as a substitute for the analysis.

Mission Class	Class A	Class B	Class C	Class D
<b>Parts Stress and Derating Analysis</b>	Required	Required	Required†	Recommended
<b>Worst Case Circuit Analysis</b>	Required	Required*	Not Required	Not Required
*Required for circuits determined to be susceptible to End-of-Life (EOL) degradation				
†Required for critical circuits				
‡Transient electrical stress analysis not required				

- The analysis check list becomes little to no WCCA, just limited stress & derating analysis

Point of Load Switching Regulator WCCA	Point of Load Switching Regulator WCCA
Specifications, Requirements, Design Objectives	Specifications, Requirements, Design Objectives
MODULE 1 - High Priority Analysis	MODULE 1 - High Priority Analysis
Stability	Stability
Conducted Susceptibility	Conducted Susceptibility
Output Ripple	Output Ripple
Switching Frequency, Duty Cycle	Switching Frequency, Duty Cycle
Startup Times, Overshoot, Inrush, Shutdown	Startup Times, Overshoot, Inrush, Shutdown
Load Step or PDNAC Impedance (< 3.3V and/or Digital Load)	Load Step or PDNAC Impedance (< 3.3V and/or Digital Load)
Voltage Regulation	Voltage Regulation

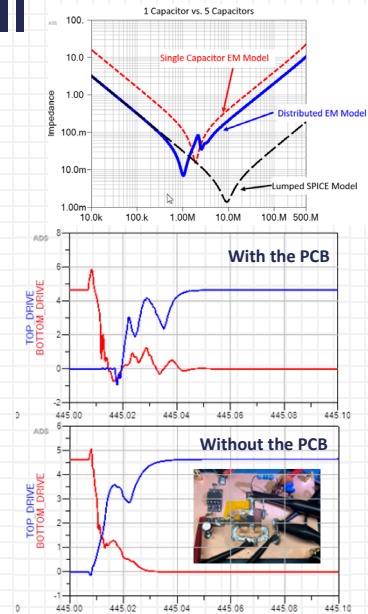
Programs often arrive at near-zero WCCA through a predictable chain of events. Requirements are vague, the analysis scope is not well defined, and the bid is created before the schematic or functional block content is fully understood. Schedule pressure, budget limits, design churn, and outdated guidance then push the team toward the smallest possible analysis effort.

Reliability analysis may not be explicitly bid, or it may be bid by someone who does not understand the technical scope. By the time CDR approaches and deliverables are due, there is often a scramble to fit analysis into a budget that was never sized correctly. The result is that what should have been a meaningful set of targeted WCCA activities becomes only a few limited analyses plus basic Stress & Derating.

Test, heritage, designer concerns, prior analysis, and known soft spots should all inform the final analysis plan, but they cannot replace the plan itself. The lesson is that WCCA expectations must be defined at PDR, before budget and schedule realities force the program into inadequate verification.

## It's About to Get Tougher Still

- **Less analysis is going to hurt more**
  - ❖ Voltages margins ↓ Currents ↑
- **Most companies can't test the power systems designed**
  - ❖ No access
  - ❖ No VNA, Invalid test setups, lack of knowledge
- **GaN/PI require EM sims and better equipment**
  - ❖ Analysis needs to include the PCB
  - ❖ Parts must be measured to make valid models
  - ❖ Higher edge speeds invalidate much of the test equipment
  - ❖ Analog Simulation Costs are Going UP
- **Real-time Power Supply Architectures - digital control likely invalidates simulation approaches**



The technical environment for power analysis is becoming more demanding as voltage margins shrink and dynamic currents increase. In many new systems, a traditional five percent voltage window may not be adequate; three percent or tighter regulation is becoming more common. At the same time, high-current digital loads, GaN devices, faster edge rates, and dense layouts require better modeling and better test equipment.

Many companies do not have the tools needed to properly test distributed power systems, such as high-bandwidth oscilloscopes, VNAs or FRAs, and suitable impedance and high-bandwidth probes.

Power integrity and GaN assessments increasingly require the PCB to be included in the simulation, which means simple free SPICE tools **produce misleading and inaccurate answers**. Vendor models are often not accurate enough for output impedance or PDN simulations, and capacitor models may not be properly de-embedded from test fixtures.

More advanced tools with electromagnetic and 3D field-solving capability are critically needed, increasing cost and schedule pressure. Finally, real-time digitally controlled power architectures may further reduce the usefulness of traditional analog simulation approaches.

## Model Trouble - PSpice/LTSpice Encryption Broken

### A Copy-Paste Bug That Broke PSpice® AES-256 Encryption

March 18, 2026 ~5 min read


<https://itsylve.blog/post/2026/03/18/PSpice-Encryption-Weakness>  
 Github - <https://github.com/itsylve/spice-crypt>  
<https://github.com/itsylve/spice-crypt/blob/main/SPECIFICATIONS/pspice.md>  
<https://github.com/itsylve/spice-crypt/blob/main/SPECIFICATIONS/ltpspice.md>

- **All past (encrypted) models are now exposed**
  - ❖ PSpice since 2006 (PSpice 15.7), 256-Bit 2014
  - ❖ Files with \$CDNENCSTART encryption
  - ❖ LTSpice .sub files and other binary files
- **Will create uncertainties about model availability**
- **Analysts will likely need to make more of their own models**

**Root Cause**

The names `g_desKey` and `g_aesKey` are reverse-engineered labels, not original source names. The key sizes suggest the extended key was intended for AES and the short key for DES. The short key is 8 bytes after derivation, matching a DES key size. The extended key is 31 bytes plus a null terminator to fill 32 bytes, which is likely an off-by-one error since AES-256 requires 32 bytes of key material. Passing the short key to the AES engine appears to be a copy-paste error from the DES code path. Had the extended key been used, the effective keyspace would be  $2^{216}$ , making a brute-force attack infeasible.

AES-256 encryption support was introduced in PSpice 16.6 (April 2014), alongside the existing DES-based modes. The bug has presumably been present since that release. Fixing it now would break compatibility with every encrypted model created in the twelve years since its introduction.


10
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The reported break in PSpice and LTSpice model encryption creates a new challenge for the analysis community.

Encrypted SPICE models have historically allowed vendors to distribute useful simulation models while protecting proprietary intellectual property. If those models can now be exposed, vendors may become more reluctant to provide detailed models or may limit what they distribute.

That would make WCCA harder because analysts depend on credible models to assess stability, transient behavior, impedance, and stress conditions. The likely result is that analysts will need to create more custom models or validate vendor models more aggressively through measurement. This adds cost, schedule, and technical uncertainty to an already difficult analysis process. The issue also reinforces a broader point: simulation results are only as good as the models behind them. Programs should plan for model development, model validation, and measurement support as part of the WCCA scope.

This is another reason AEI has focused on model development and brings all the modeling building skills as well as a significant library of modeled devices to each project we work on.

## What's the #1 Design Issue WCCA Finds?

- **Hands down – Power Integrity (PI)**
- PI has been the number one design **FAILURE** since we started looking at it and nothing else is close
- **AC Power Plane Impedance is not meeting target impedance and Q**
- **Why its critical - SI is the Goal, PI is the Foundation**
- Impacts so many things
  - ❖ Good PDN design is critical to ensuring clean power, good signal integrity performance, and meeting EMC/EMI limits
- **Shockingly, PI analysis is often not performed AT ALL or even tested**

**Power → Load**

**Many designs fail here!**

What's your plan for PI? Target Impedance?  
Do you own a VNA?  
NG SME "requirements are DC only" 🤔

Level of ignorance is astonishing - pervasive

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11

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The #1 design issue AEi finds in WCCA is power integrity. The most common failure mode is that the AC power plane or PDN impedance does not meet target impedance and/or has excessive Q.

Power integrity affects regulation, signal integrity, EMI/EMC performance, timing, noise margin, and overall system robustness. The phrase “signal integrity is the goal, power integrity is the foundation” captures the relationship: poor power delivery can make otherwise good high-speed interfaces fail. Many organizations still do not perform power integrity analysis or even test impedance, despite the increasing dynamic current demands of modern FPGA, ASIC, and processor loads. The problem is often cultural as much as technical, with requirements focused on DC behavior while the real risk is dynamic AC behavior. Every program should have a clear power integrity plan, a target impedance strategy, and the ability to measure or analyze whether the design meets it.

Some of the Videos Available at AENG.COM

**How-To Design for Power Integrity Series**

<https://www.youtube.com/playlist?list=PLtq84kH8xZ9FNXAsf-odoGNe6h5A6D3in>

**The Unfortunate State of Power Integrity in Space Systems**

<https://www.youtube.com/watch?v=crLZTirpeXs>

**How2Power Series, Troubleshooting Power Distribution Systems**

<https://web.how2power.com/videos/index.php>

**Webinar: Flat Impedance in Voltage Regulator Modules**

<https://www.youtube.com/watch?v=eOXzK-1WQ24>

**Power Integrity Ecosystem by Heidi Barnes from Keysight – Dgcon 2017**

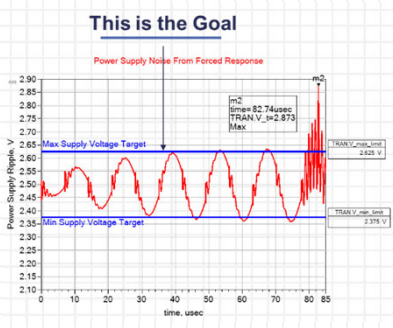
<https://www.youtube.com/watch?v=NrxMtTgJhfE>

<https://www.keysight.com/us/en/library/demos/demo/power-integrity-ecosystem-by-heidi-barnes-from-keysight-2883724.html>

## DC Regulation Often Fails To Meet Limits

Type	Regulator	DC Value (V)	DC Regulation Range BOL EVA	DC Regulation EOL RSS-EVA	DC Regulation EOL EVA-EVA	Aging (Year)	Radiation TID (krad)	With Transient Effects Included
DC/DC	SVRTR2805S	5	2.20%	1.82%	3.20%	17	30	11.70%
DC/DC	SVRCH283R3S	3.3	-6.52% - 7.277%	-8.973% - 7.488%	-10.217% - 8.732%	17	30	-13.429% - 11.944%
DC/DC	SVRFL283R3S	3.3	1.29%	1.29%	1.76%	5	1.5	14.55%
Switcher	TPS50601A	3.301	3.32%	-5.474% - 5.195%	-6.932% - 6.654%	17	30	??
Switcher	TPS7H4003	0.907	-2.104% - 1.773%	-2.641% - 2.51%	-3.016% - 2.685%	5	1.5	??
Switcher	TPS7H4010	3.308	-2.184% - 1.57%	-3.261% - 2.647%	-3.558% - 2.944%	5	1.5	??
Switcher	TPS7H4001	0.953	0.937V - 0.966V (-1.674% - 1.344%)	0.934V - 0.971V (-2.024% - 1.859%)	0.934V - 0.971V (-2.044% - 1.879%)	15	100	??
POL	ISL70001	1.8V	3.28%	4.83%	7.27%	20	100	??
POL	ISL70002	1.1V	3.49%	4.04%	6.63%	20	100	??
LDO	TPS7A4501	1.805	-3.762% - 5.062%	-3.797% - 6.276%	-6.068% - 8.547%	17	30	??
LDO	TPS7H1101A	3.293	2.71%	2.69%	5.99%	15	100	??
LDO	LM117	11.771	3.35%	-5.733% - 8.14%	-7.65% - 10.058%	15	100	??
LDO	RHF14913	4V	6.92%	7.49%	11.78%	42	1000	??
LDO	ISL75052	1.112	2.69%	3.70%	6.15%	15	9.8	??

- Many regulators don't make 5% DC regulation WC EOL
- Dynamic headroom is impacted and not assessed



The regulator examples show that many power supplies do not meet a five percent worst-case end-of-life DC regulation requirement. This is important because the allowable operating voltage range for a load is not reserved only for DC regulation error. The same voltage window must also include ripple, transient response, IR drop, PSRR effects, load-step behavior, aging, radiation, and other noise sources. If the regulator itself consumes most of the allowable margin, little or no margin remains for dynamic current effects.

Dynamic headroom is often not assessed, even though it may determine whether the load actually operates within its required voltage limits. The table demonstrates that both DC/DC converters and LDOs can have much larger worst-case excursions than expected. This reinforces the need to analyze each rail as a complete power delivery system rather than as an isolated regulator data sheet value. Programs should not assume that meeting nominal output voltage is equivalent to meeting the load's real operating voltage requirement.

# Power Distribution System

**Meeting the Requirements of the Load is Key FOR EACH POWER RAIL:**  
**EOL DC Regulation + PSRR + IR drop + Ripple + Step Load**  
**< Recommended Voltage Range, often 5% or less**

**Power Supply IC Manufacturers**      **Power Supply Designer**      **Digital Designer**

**Where does the responsibility lie?**

**PS Impedance = Plane/load Impedance**

**What beads do to PDN impedance**

**What About Dynamic Current?**

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A power rail must be assessed as a full distribution system, from the power supply through the PCB plane and decoupling network to the load. The load's recommended voltage range must include end-of-life DC regulation, PSRR effects, IR drop, ripple, and step-load transients. WCCA reveals that most power ICs already use a large portion (> 3%) of the allowable 5% voltage window, leaving little room for dynamic load transients (dynamic headroom).

The PDN impedance determines how much voltage disturbance occurs when the load current changes, especially at resonance frequencies. These resonant disturbances may not appear in a simple bench test, but they can still cause major operational problems in the field. Responsibility is often unclear among the power supply designer, the power IC manufacturer, and the digital designer, but the load requirement must ultimately be met by the system. The right question is not whether the regulator works in isolation, but whether the complete rail meets the load requirement under worst-case conditions. WCCA and PI analysis provide the framework for answering that question.

# Power Integrity Fails

**100 engineers surveyed**  
**Why did you add a bead?**  
**Survey says #1 answer**  
**“vendor told me to”**

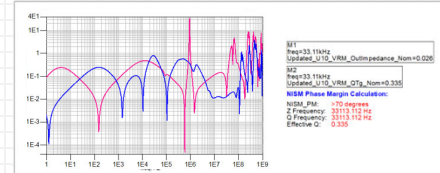
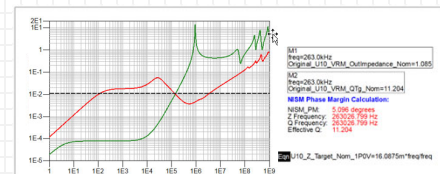
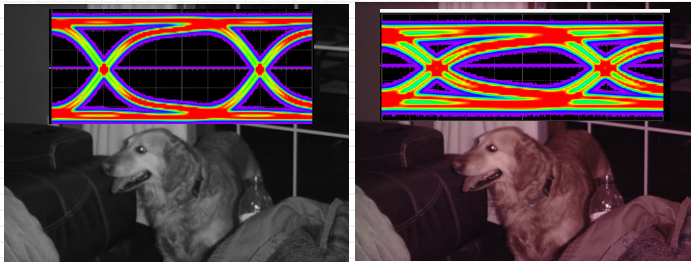
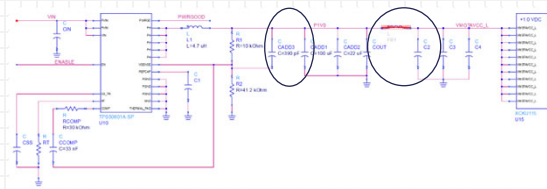
14
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This slide highlights a common power integrity failure pattern: components such as ferrite beads are added because a vendor or reference design recommends them, not because the system impedance has been analyzed. Ferrite beads can create resonances with decoupling capacitors and power planes, especially when used on high-speed digital rails. Those resonances can amplify noise instead of attenuating it, creating exactly the problem the bead was intended to solve. Examples such as Ethernet PHYs, LVDS interfaces, and FPGA power rails show that these are practical design issues, not theoretical concerns.

The lesson is that power integrity design cannot be based on rules of thumb alone. Every bead, capacitor, plane segment, and regulator output impedance should be evaluated in the context of the actual PDN. Reference designs may be useful starting points, but they must be verified against the mission-specific load, layout, and operating conditions. Blindly copying vendor recommendations can create hidden resonances and soft failures that are difficult to diagnose later.

## Power Integrity Fails

- Noise concern with camera sensor
- Cold temp raises noise floor
- Cold temp degrades PS stability
- Noise closes eye
- Leads to 'soft' failures



Power integrity failures often appear as soft or intermittent failures rather than obvious hard faults. In the camera sensor example, noise concerns are worsened by cold temperature, which raises the noise floor and degrades power supply stability. The resulting noise can close the eye diagram and reduce signal margin, leading to degraded or unreliable performance. These failures may be difficult to reproduce because they depend on temperature, operating mode, load activity, and the exact impedance behavior of the power distribution network. A design can pass a limited functional test and still fail under realistic dynamic or environmental conditions. This is why power supply stability, impedance, and noise behavior must be analyzed across worst-case conditions.

The slide also shows how power integrity interacts directly with signal integrity: a noisy rail can degrade the quality of the data path. WCCA helps expose these coupling mechanisms before they become intermittent field failures.

## Need to Define Expectations at PDR

- **Better Analysis/Test Planning at PDR**
- **Targeted WCCA should be performed based on SME reviews**
  - ❖ Follow TOR-2013-00297 – Use Functional Block Analysis Checklists
  - ❖ Buyers need to adopt Checklists
- **Account for Testing Deficiencies, Fills the Hole with Analysis**
- **Can't ignore WC stress including transient stress – Best Expenditure of Analysis \$\$**

### Takeaways

- **Use Intelligent Rigorousness – Analyses is not all or nothing**
- **We desperately need to learn to test impedance**

The best time to define WCCA and test expectations is at PDR, when functional blocks are known and there is still time to influence the design. A targeted WCCA plan should be based on subject matter expert review, functional block checklists, requirements flow-downs, derived requirements, and known design risks. The analysis plan should start broad, using established checklist guidance, and then be reduced intelligently based on risk, test coverage, heritage, and priority. This is the idea of intelligent rigorousness: analysis is not all or nothing, and the right level of rigor depends on the design and mission risk.

A pre-WCCA design review by experienced engineers is one of the most cost-effective ways to find nominal problems and likely tolerance-stack issues early. Test deficiencies should be identified explicitly so that analysis can fill the gaps rather than assuming test will cover everything. Stress & Derating analysis should not be reduced to static math only, because transient stress is often the real circuit killer. Programs also need to learn to measure impedance, because power integrity cannot be managed without understanding the PDN.

## Call to Action: Power Integrity Track Needed

- 2017 – The Unfortunate State of Power Integrity in Space Systems
- 2021 – Power Integrity Challenges, An Update
- 2026 - Have We Forgotten What Works?
  
- Still no PI track but we are flying AMD Versals and we want AI in Space
  
- When will we realize that Power Integrity needs to be understood and seriously addressed by the space community?
  
- **100% of the designs we review have PI problems**

The space community has been warned about power integrity problems for years, yet the industry still lacks a dedicated forum or track focused on low-voltage, high-dynamic-current power systems. Prior presentations in 2017 and 2021 raised the issue, and the 2026 message is that the problem has not gone away. In fact, it is becoming more urgent as space programs fly advanced devices such as AMD Versal-class processors and pursue AI workloads in orbit.

These systems cannot be supported reliably by legacy power design assumptions or DC-only requirements. The statement that 100 percent of reviewed designs have power integrity problems is intended to emphasize how pervasive the issue has become. Without dedicated education, standards, test methods, and design guidance, each program is left to relearn the same lessons. A power integrity track would help bring the space community together around target impedance, PDN measurement, modeling, decoupling, stability, and dynamic load verification. The call to action is to treat power integrity as a core mission assurance discipline, not a specialty topic.

## Bio

- Supporting Space programs with WCCA for more than 30 years, Independent WCCA SME
- AEi Systems CEO since 2001, Established leader in analysis, modeling, and troubleshooting of high reliability systems
- **Contributed key portions of Aerospace TOR-2013-00827 Electrical Design Worst-Case Circuit Analysis Guidelines Standard** (2012, 2013)
- Picotest Test Equipment since 2010
- Co-Founded Intusoft – SPICE Company



18

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### Abstract: "Worst Case Circuit Analysis: Have We Forgotten What Works?"

As space systems grow more complex under tighter budgets and schedules, many programs are drifting away from proven mission assurance practices—driving increased reliance on test, reduced analytical rigor, and greater risk. Ignoring lessons learned is not the optimum path.

With constrained engineering resources, expanding use of reference designs, and new technology challenges, the need for targeted Worst Case Circuit Analysis (WCCA) and Stress & Derating analysis is greater than ever. These time-tested methods remain essential for identifying and reducing both day one and EOL risk.

This presentation highlights a concerning trend: analysis is being minimized or eliminated, often replaced by incomplete test strategies and unclear expectations. We'll also examine challenges in scope definition, emerging technology pressures, and the continued impact of poor power integrity design practices on mission reliability.

#### Topics Covered:

1. The Current State of Battle for Reliability
2. What WCCA/Stress Find
3. Data Item Description Challenges
4. How Programs End Up with Near Zero Analysis
5. Near Term Analysis Challenges and Drivers
6. Test Deficiencies, How Analysis Fills the Gaps
7. PDR – A Time to Define Expectations
8. The #1 Design Issue We See
9. Recent Power Integrity Fails
10. Call to Action: Power Integrity Track