BLOG 5: Too Many Escapes and Biases

"Escapes" is a euphemism for all the excuses programs, program managers, engineers, and reviewers use to curtail or eliminate WCCA associated activities. It is essential that all the elements noted in the (first) Going It Alone blog section, necessary to perform the WCCA, be brought together along with the right software, people, test data, and experience. With each hurdle, the analysis will stall, impacting the level of rigorousness, and the veracity of the conclusions.

In addition, there are a variety of issues that can plague a successful completion of WCCA. Here is a list of some of them.

Some common Escapes are:

- Lack of budget or foresight to properly scope out and budget the effort
- Poor, non-existent, or ever-changing design specifications or flowdown requirements from the customer
- We test (see below)
- We have redundancy – Note: redundancy won't save a bad design
- Time compression or poor scheduling
    - WCCA needs time. WCCA is often force fit between the end of the design process and production. Unfortunately, too many programs find themselves still designing right up until final reviews or after WCCA findings are revealed and there is little or no time to properly perform the WCCA let alone fix the issues found. WCCA needs time to be completed properly and any non-compliances addressed appropriately. A reanalysis pass to define and confirm fixes is **ALWAYS** necessary.
    - WCCA needs test data to support models and assumptions, if the hardware does not meet up with the analysis, problems will occur
    - The need for hardware is essential for efficient WCCA. The lack of part data to fill in datasheet holes, model correlation data to bound and define model performance, and circuit correlation data to anchor simulations, assummptions, and conclusions is so critical. Without it you will be making judegements and design decisions without a firm foundational basis
- Designers who think they don't need to do the analysis
    - The selection of the parameters to be analyzed should NOT be generated by the circuit designer alone. Mistakes in the design will often be repeated in the analysis. Circuits that the designer believes are too simple, obvious, or heritage may be ignored. This is often where problems lie.
    - Underestimating the Tolerance Stack-up. Until the tolerance database ('PVDB' - Parts Variability Database) is compiled AND the analysis performed it is tremendously difficult to know what part tolerances will do to performance. We know so very little about the parts we use. And we often do not know the sensitivity of the circuit performance to various unbounded or undocumented parameters. To dismiss the variances as inconsequential before performing the analysis is one of the biggest escapes. Whether RSS'd or EVA'd, the tolerance stack-up is bigger than you believe it to be.
- Company, Program, and Engineering Biases - These entities often…
    - Are infected by the nominal. They believe they know all they need to know given typical data. Typical data sheet information and curves and typical test data are often used to

justify conclusions about worst case behavior, tolerance distributions, and so much more. Often the nature of the data is not even explored. Statistically speaking, the nominal does not tell you about extremes and should not be used to bound WCCA. The difference between a nominal stress analysis, a worst case steady state stress analysis and a worst case transient stress analysis (using EOL part values, loading and environment extremes) can easily be an order of magnitude.

- Believe their past success is a future predictor even if the parts, requirements, environment, and the designs change. Likely, it would be difficult to trace the issue back to a particular circuit or functional block if there were a unit failure
- Believe they have done all the homework they need to (e.g., what little analysis they do along with test data, which is both deemed accurate and sufficient, clears any functional concerns or risks)
- Put 100% stock in reference designs and data sheet information, without any hint of pessimism. (They are unfamiliar with the tolerance stack-up and the 'Cracker-Jack' phenomenon – i.e., the surprises that are waiting inside most ICs that you don't know about until you open the box and look (deeply) inside)
- Do not understand the role limited, priority based, and targeted WCCA can play in achieving higher reliability and meeting mission performance goals and do not care to learn how it can benefit them.

- It costs too much or we don't have anyone to do it – clearly these escapes bely reality. As for cost, WCCA doesn't cost money. It saves money. This may seem misguided at first, but once you understand the direct and ancillary benefits it's easy to see. Below are just a few. Planned and executed well, the costs can be managed. As for who can do the work, well, consultants exist and the work can be targeted.

Reasons to Perform Worst Case Analysis

Need	Reason
Design Verification and Reliability	To verify circuit operation and quantify the operating margins over part tolerances and operating conditions - Will the circuit perform its functions and meet specifications/To quantify the risk
	To improve performance - to determine the sensitivity of components to certain characteristics or tolerances in order to better optimize/understand a design and what drives performance
	To verify that a circuit interfaces with another design properly
	To determine the impact of part failures or out of tolerance modes
Test Cost Reduction	To evaluate performance aspects that are difficult, expensive, or impossible to measure (i.e. determine the impact of input stimulus and output loading so as not to damage hardware)
	To set ATP limits - How else besides analysis will you know what you are supposed to see in test?
	To verify SATs/SITs and if they are needed/what their limits should be
	To reduce the amount and scope of testing
Parts Assessment	To determine if a part is suitable (too cheap, too expensive) or if a New Technology can be used
	To support/set critical parameters and SCD requirements/screening definition
	To perform Single Event Transient (SET) analyses
	To support the switching and transient Stress & Derating analysis
Schedule, Cost, or Contractual Risk Reduction	To reduce board spins - determine the impact of late stage design or part changes
	To verify changes to heritage circuits
	To obtain better insurance rates or reduce contractual liabilities
	To avoid a catastrophic or costly incident
Return on Investment	To improve future products
	To improve the knowledge and capability of your engineering staff

The ROI on WCCA is significant. Here are some of the many reasons to perform Worst Case Analysis.

"We test so we don't need to analyze"
This is one of the biggest escapes of all. Can't electrical testing be used as a less expensive alternative? The answer is generally no.

"We test and the mission is short." As noted in the **Optimizing Electronics Test/Analysis Ratio** (https://www.aeng.com/pdf/MRQW_2020_Reliability_Test_vs_Analysis_AEi_Systems.pdf) the BOL vs. EOL tolerance variances are discussed. BOL tolerances dominate. Testing does not usually account for BOL tolerances; initial testing is rarely is as extensive due to various practical constraints. So, test does not retire as much risk/margin as people think relative to the tolerance stackup.

Testing normally only determines typical 25C performance. In many cases, extended testing must be performed with extreme operating conditions such as temperature, voltage, power, etc. to determine aging margins. This can overstress the hardware. Testing is only valid for the measured lot and may vary lot-to-lot and manufacturer-to-manufacturer. It requires the parts to be procured PRIOR to completion of the WCCA, which can be very risky. And it can be very costly if many measurements or sophisticated test equipment are required.

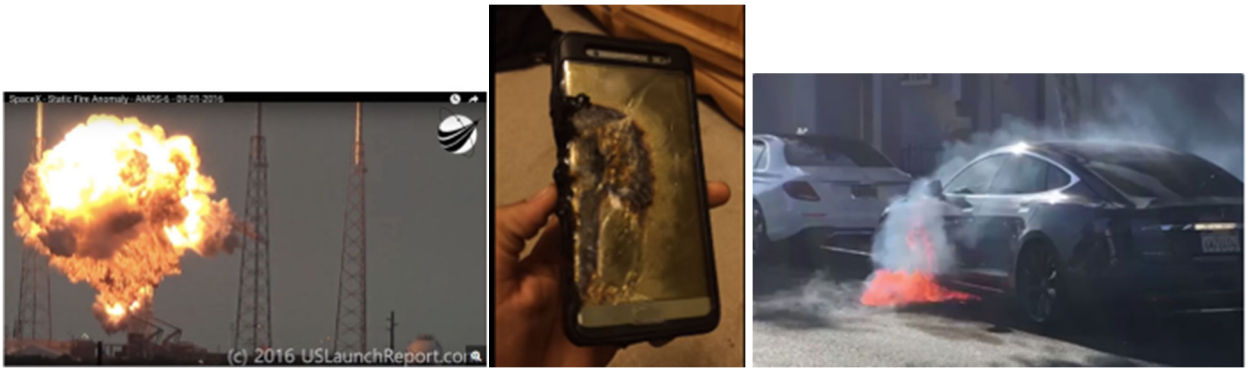
While testing is essential to support the WCCA, testing doesn't cover EOL analysis and often doesn't even cover all operating conditions. In addition, test has the following inherent concerns:

- Without analysis how do you know what you expect to see. One of the most basic rules of testing is know what you expect to see. And this is often impossible if you have not performed any analysis
- Testing isn't cheap, fast, or easy. Test setups often distort measurement data, and most labs are severely under or ill-equipped
- Testing does not compute margins, risk, or parametric sensitivity; three key outputs of WCCA. Therefore, it is much harder to improve the design with only test data as the guide
- Many of the things we need to look at are simply not tested or even testable
- Worst case test conditions are often not defined, unattainable, or would over-stress the hardware
- Testing is often limited to the top level outputs. If an anomaly isn't seen, probing to lower levels is often not performed. Key functional blocks are often not tested. For instance, it is easy for an opamp or power supply with poor stability to hide in a system that appears to be working properly. The poorly performing circuit may be masked and dismissed as increased noise. It is known that stability margins of control loops can change 20-30 degrees over temperature and life. Without knowing where you stand nominally, EOL issues can easily crop up
- The differences between engineering model and flight/production parts and layouts are often underestimated
- In many cases, the PCB can impact the performance of the circuit. Therefore, it is essential that the final layout be used when testing
- One of the places where we find the many worst case issues is in power supplies. Power supplies are often not measured down to the level they should be, and the size of today's power supplies is often so small that they cannot be measured properly or easily

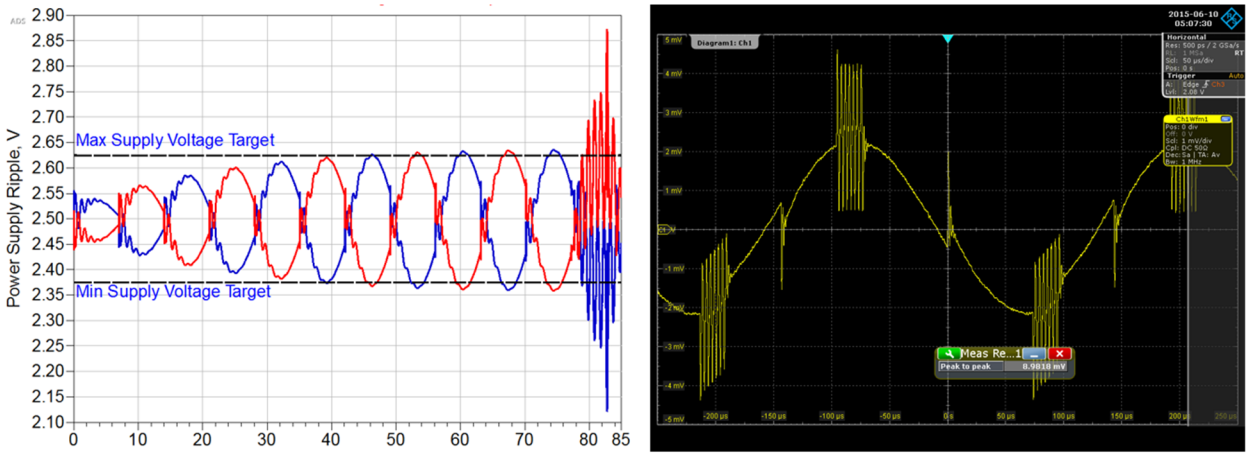
Eliminating Bias, Ensuring Independence

Why WCCA is Challenging

The project engineer is often under great schedule pressure, the program budget pressure, and the company political pressure. One of the main tenants of the Aerospace TOR guideline on WCCA (TOR-2012(8960)-4_Rev. A) is that WCCA performed in house is not independent. Monetary, political, personal feelings all serve to destroy the checks and balances that WCCA is supposed to bring to the design process. This is not to say that designers should not be involved. Certainly, the designer should develop the nominal models and be involved in the WCCA review. But independence is key to avoiding escapes. While some of these biases can influence even the most independent of analysts, this is clearly why companies and design engineers should not do their own worst-case analysis and why it is imperative to use an independent assessment team.



Rocket Explosions, Samsung Galaxy battery fire, Actress Mary McCormack Posts Video of Her Husband's Tesla on Fire.



Some images of Worst Case happening every day. Poor power integrity can lead to rogue waves (left and right). These are transient load conditions where there is an alignment of the stepped current requirements of the load (FPGA, processor, memory) and resonances in the power rail's PDN impedance. When this happens the power supply voltage can jump out of specification resulting in a fault condition. This is tremendously difficult to recreate in traditional production testing. But this worst case event happens all the time in real life.