CS5308 TWO-PHASE BUCK CONTROLLER

1.0 Scope

The purpose of this analysis is to model the CS5308 Two Phase Buck Controller with Integrated Gate Drivers.

Analysis:	Two-Phase Buck Controller modeling
Last Rev Date:	5-9-2002
Publication Number:	CS5308/D
Revision	March 17, 2005
SPICE File	CS5308.LIB

2.0 Functional Description

The CS5308 is a two-phase buck controller with four integrated gate drivers intended to drive two half-bridges, Phase 1 and Phase 2. The two phases are ±180° out of phase. Each phase has a separate current sense input (CS1, CS2), but all the outputs have common voltage feedback and compensation / soft start inputs. The current sense inputs are connected to two current sense amplifiers, and their outputs are added together. The sum is used to turn all the outputs off whenever the total current exceeds the current limit setting (ILIM). The controller also has a 5-bit DAC. The DAC output is connected to the non-inverting input of the controller error amplifier. The output voltage of a buck converter can be programmed to 32 levels. In addition, the controller has Under Voltage Lockout for VCCL and VCCH1. Power-good and VTT monitoring is provided. The CS5308 is similar to the CS5322 with some exceptions noted below.

3.0 Assumptions and Comments

The CS5308 differs from the CS5322 as follows:

1. An internal voltage ramp is added to each PWM input. At 50% duty cycle, the ramp reaches 125mV. The slope is adjusted to track the switching frequency (If 100% duty cycle is reached, the ramp will stop rising when it reaches 375mV and remain there until reset).
2. VTT monitoring with delay timing is provided. The VTT input threshold is 1.05V. The VTTCT charging current is proportional to switching frequency in accordance with fig. 4 of the manufacturer's data sheet.
3. The VTT GOOD logic output shuts down the converter when it's set to logic low, however, the threshold voltage at which this occurs is not specified on the data sheet. The threshold is set to 1.25V, similar to other logic pins on the device. If desired, It can be easily adjusted by changing EB10 (V(17) if statement): change 1.25 to new value.
4. The DAC input truth table is different, and agrees with the VID table in the manufacturer's data sheet. The voltage range is slightly different as well, offset by 25mV lower.
5. Fast feedback directly from VCORE is added to the PWM inputs. CSREF is added to the PWM inputs instead of VFB.
6. The soft start feature and frequency compensation have been combined so that only one connection to the COMP pin is required. The CS5322 has a separate and independent soft start.
7. The current limit amplifier gains for CSA1 and CSA2 are 3.5 instead of 3.15. AVPA gain is 1.86 instead of 2. The pulse by pulse current limit threshold (input to MAXC1 and MAXC2) is 0.4V instead of 0.33V.
8. Apparently, there is an error on the manufacturer's data sheet that should be corrected. The pulse by pulse current limit at the input, V(CSx) – V(CSREF), is specified at 105mV nominal, the same as the CS5322. The other changes mentioned above suggest that this should be changed to 114.3mV. This is particularly important if the min and max values are similarly affected and should be corrected on the data sheet. The higher current limit value could cause increased component stress and ultimately lead to higher failure rates of the end users' products.
9. The PWRGD threshold is +/- 12% instead of +/- 11%.
10. The gain for VDRP is 0.91 instead of 1.

11. The VCCL start threshold is 4.3V instead of 4.4V.
12. The VCCL stop threshold is 4.1V instead of 4.2V.
13. The VCCH1 start threshold is 8.5V instead of 2.0V.
14. The VCCH1 stop threshold is 8.0V instead of 1.8V.

There are some issues with the application circuit shown in the manufacturer's data sheet that would make it take very long to simulate (refer to mfr's fig.1). The SPICE model for this circuit differs as follows:

15. Rcmp1, Ccmp2 have been deleted, Ccmp1 is connected directly to GND. This shortens the soft start time. There is a bit of current overshoot during start up. Increasing Ccmp1 could reduce this (at the expense of longer simulation time).
16. Cref was changed from 0.1u to 0.01u. This avoids premature current limiting during start-up.
17. VCCL12 is connected to 5V not 12V to improve simulation time.

4.0 SPICE Model

PSpice was used to model the device. The schematics and netlists were prepared using OrCAD Capture version 9.23 and Microsim Schematics version 8.0

5.0 SPICE Simulations and Analyses

The model was simulated and the results were compared to the manufacturer's data sheet. The Spice test circuits and simulation results are shown below.

5.1 D/A Converter Output

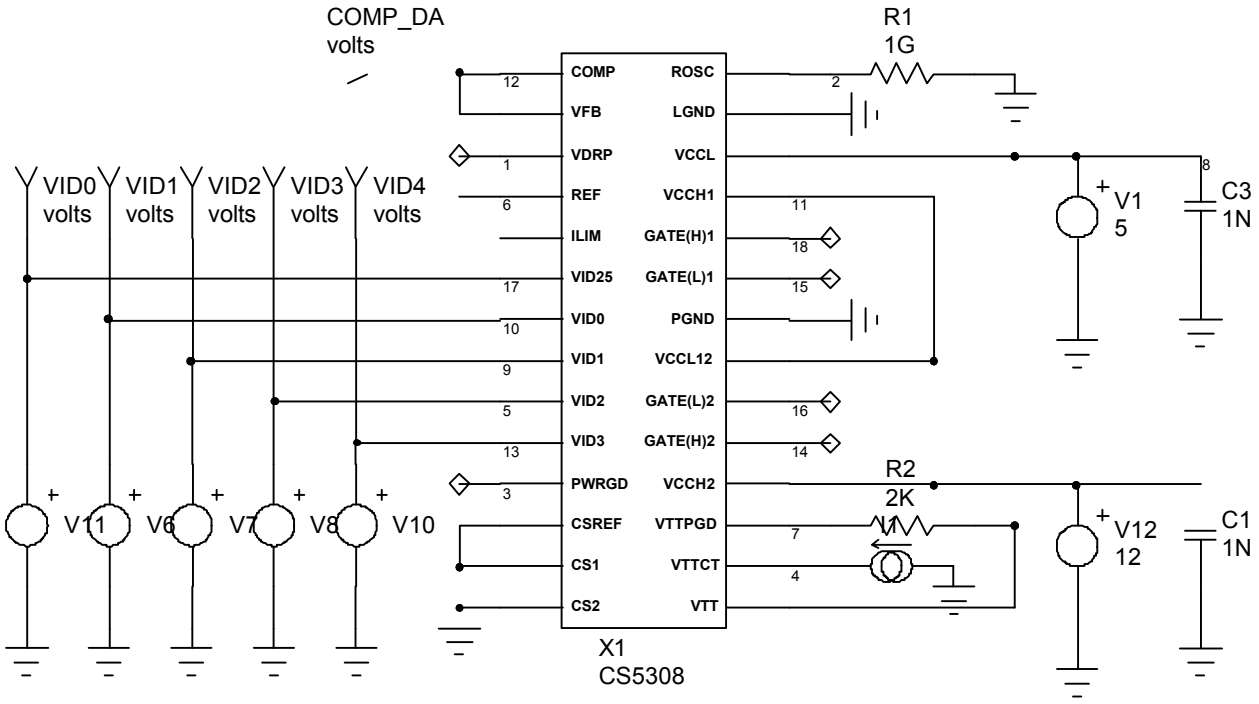

Figure 5.1.1 DAC Spice schematic

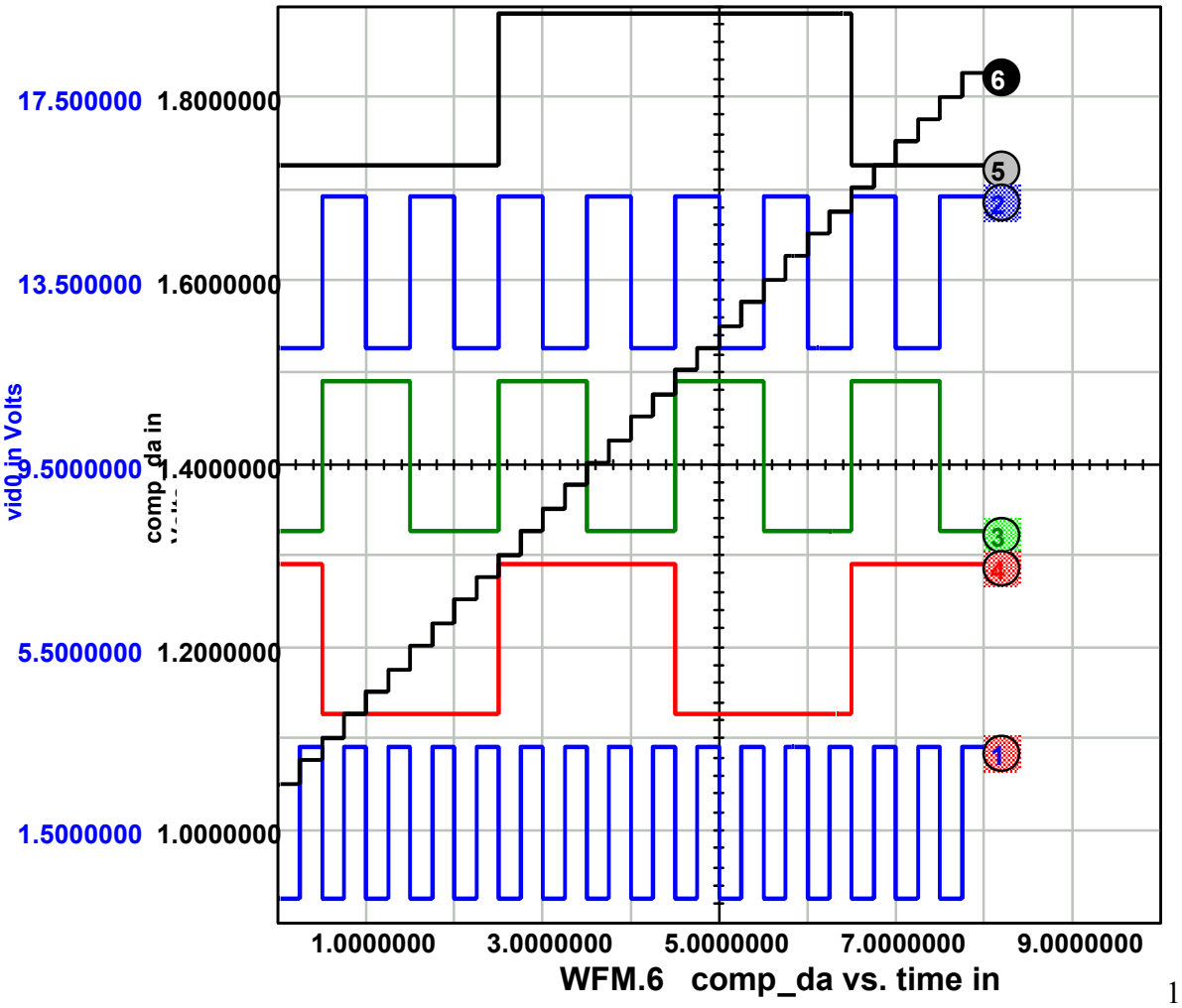

Figure 5.1.2 DAC Output SPICE Waveforms

5.2 POWER GOOD Output

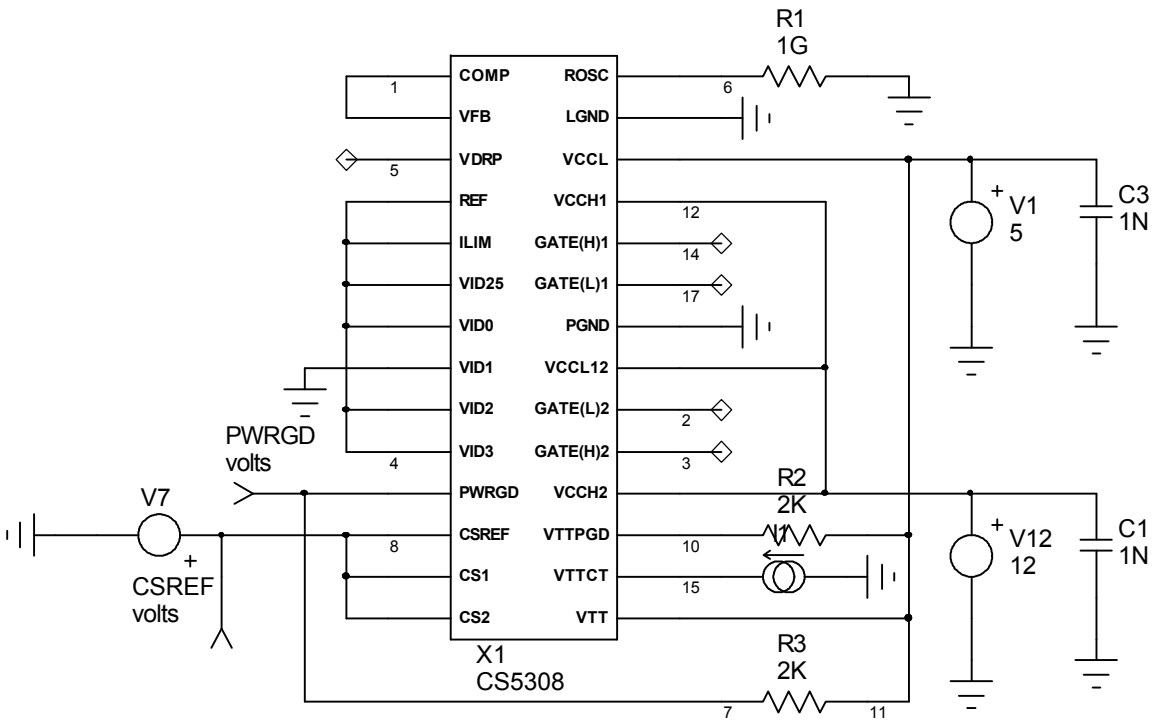

Figure 5.2.1 POWER GOOD SPICE Schematic

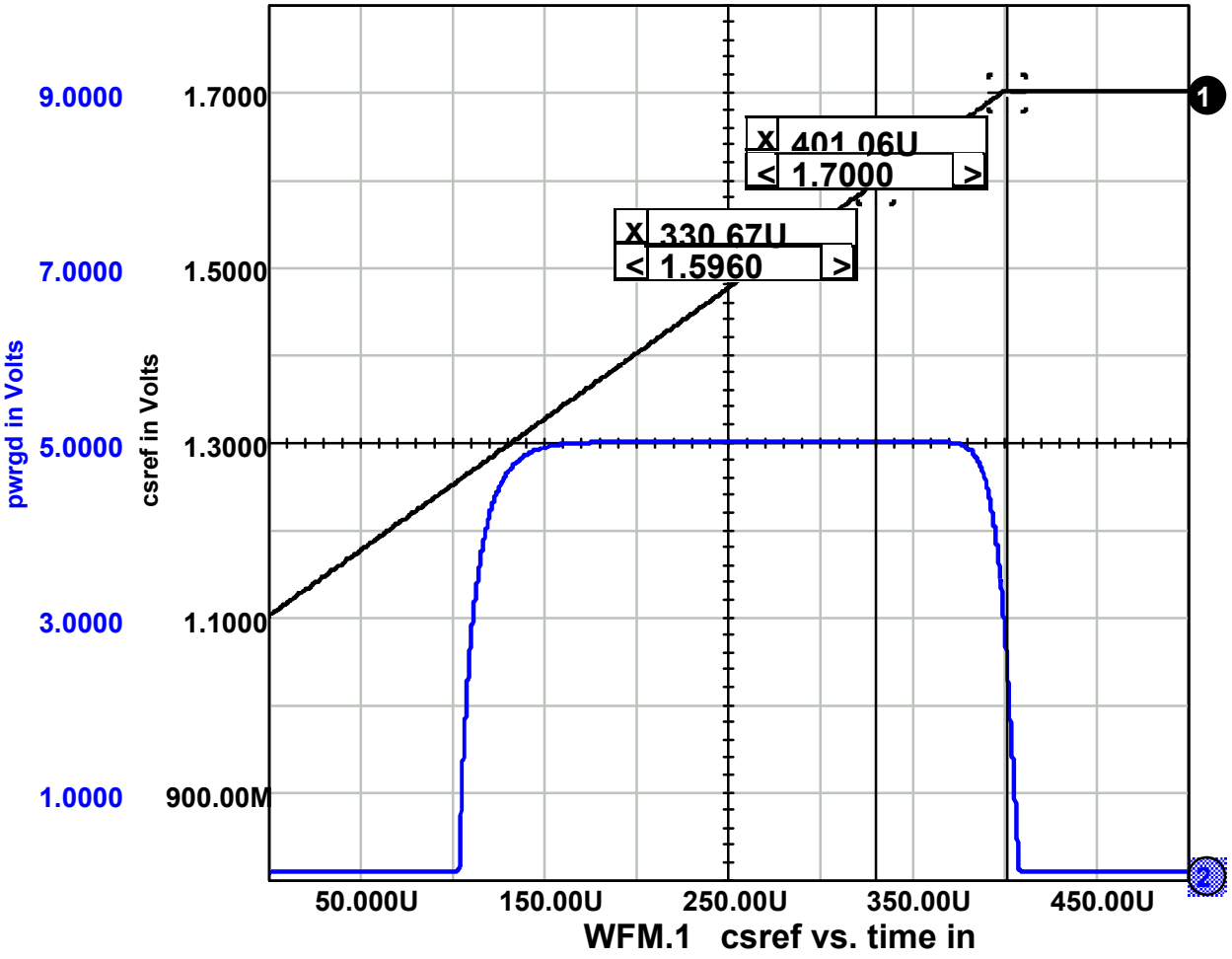

Figure 5.2.2: Power Good Spice waveforms

5.3 VTT GOOD Output

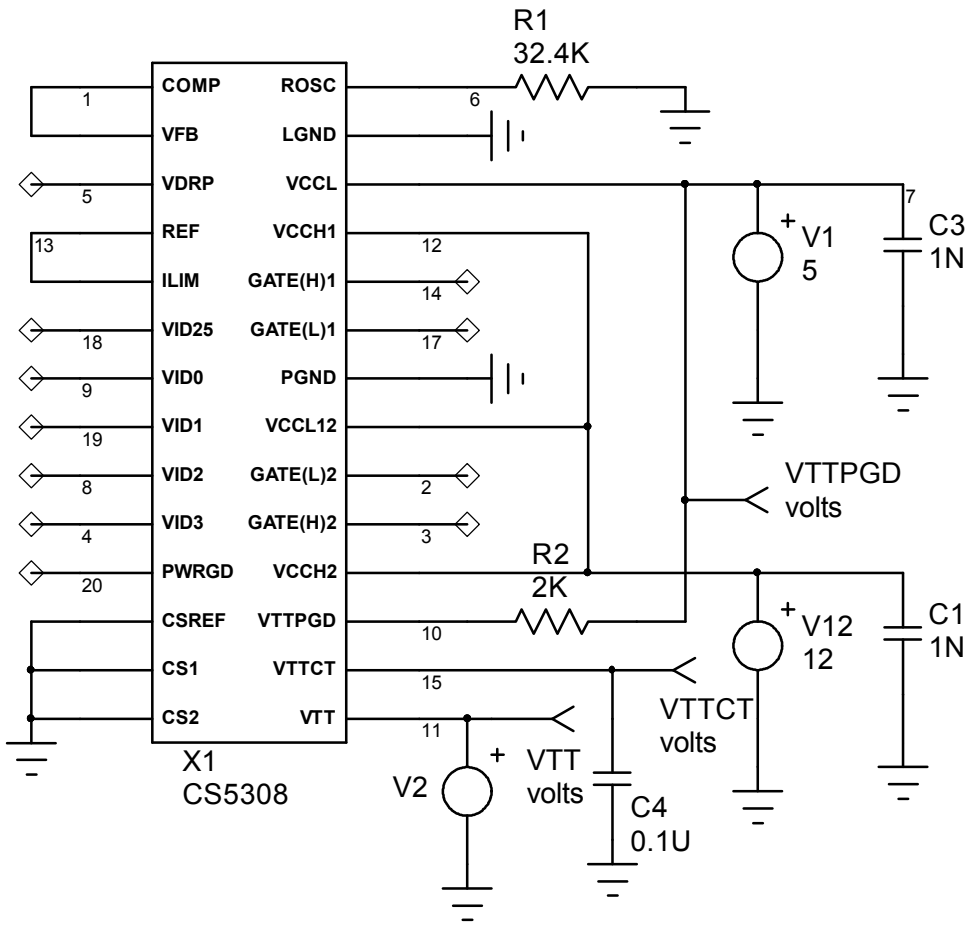

Figure 5.3.1 VTT GOOD SPICE Schematic

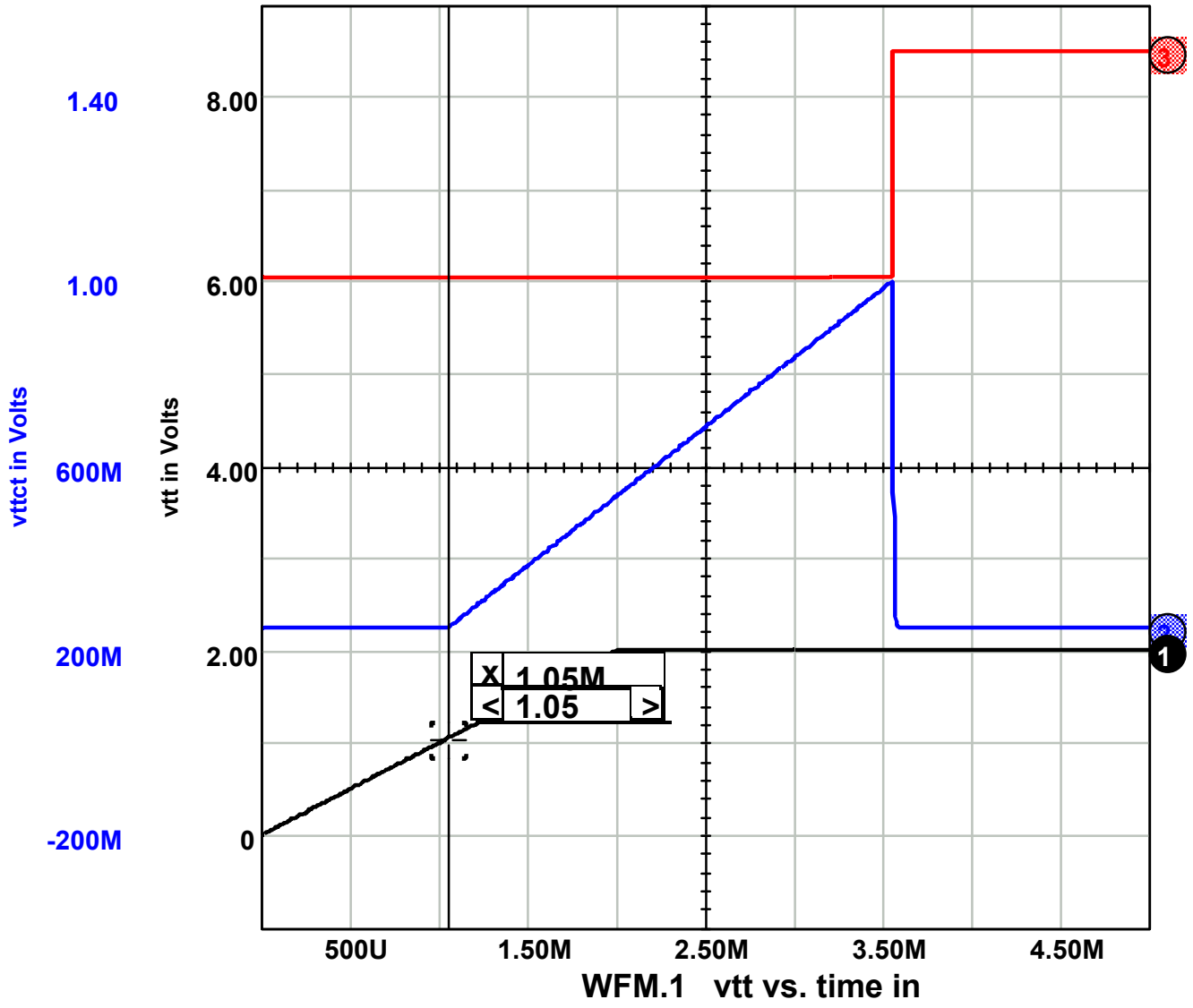

Figure 5.3.2 VTT GOOD SPICE Waveforms

5.4 Application circuit

The CS5308 model was also tested in the application circuit found in fig. 1 of the manufacturer's data sheet and shown below:

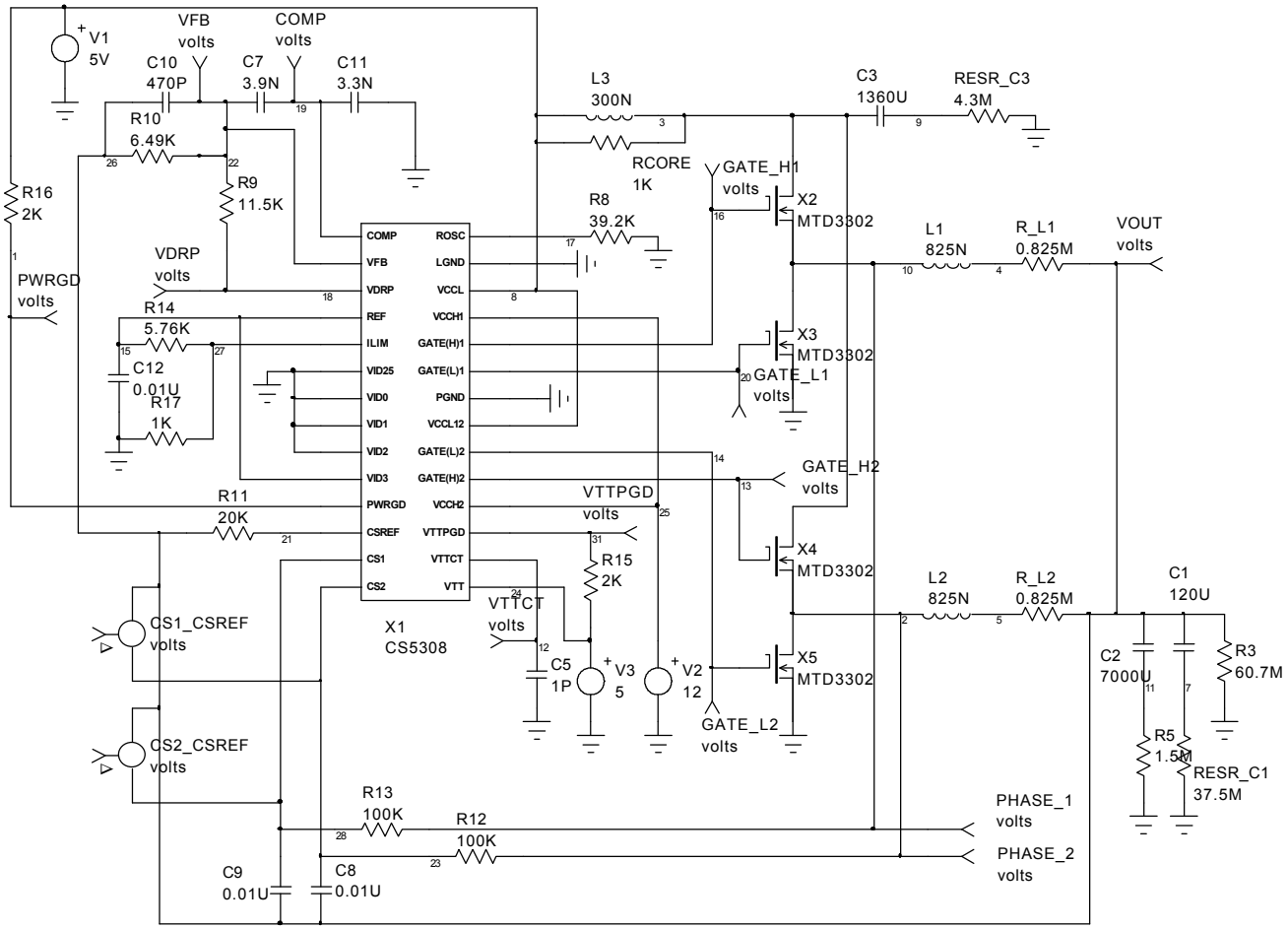

Figure 5.4.1: 5V to 1.7V/ 28A at 335kHz with 12V Bias Spice Application

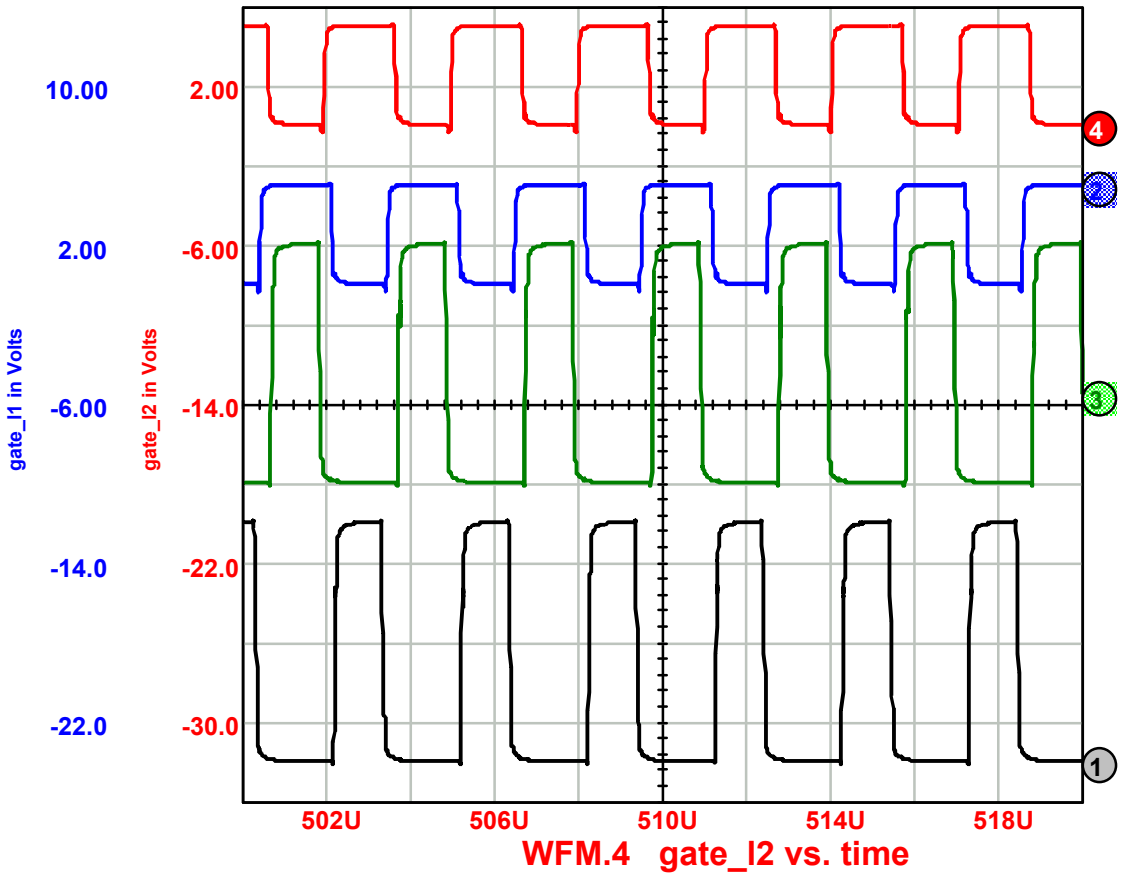

Figure 5.4.2 Spice Application Output Waveforms

Top to bottom: GATE(L)2, GATE(L)1, GATE(H)2, GATE(H)1

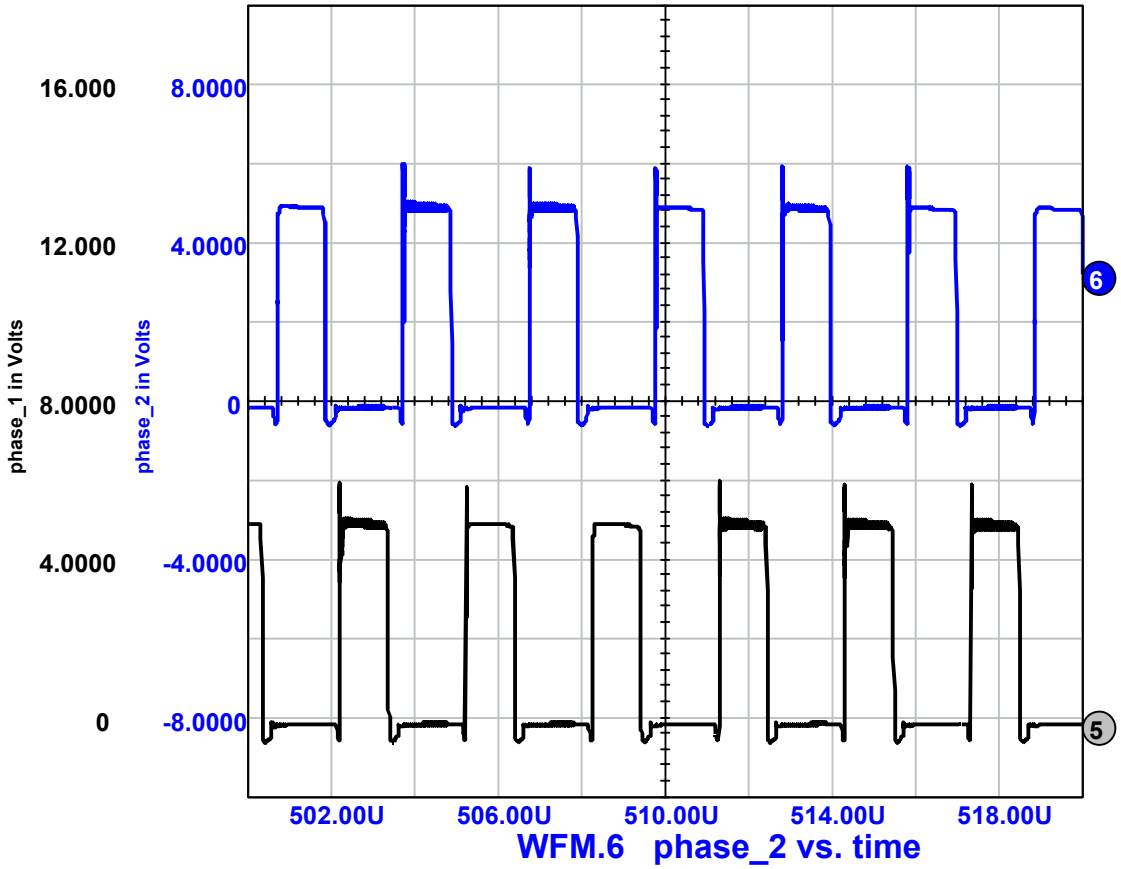

Figure 5.4.3 Spice Application Output Waveforms

Top to bottom: PHASE2, PHASE1

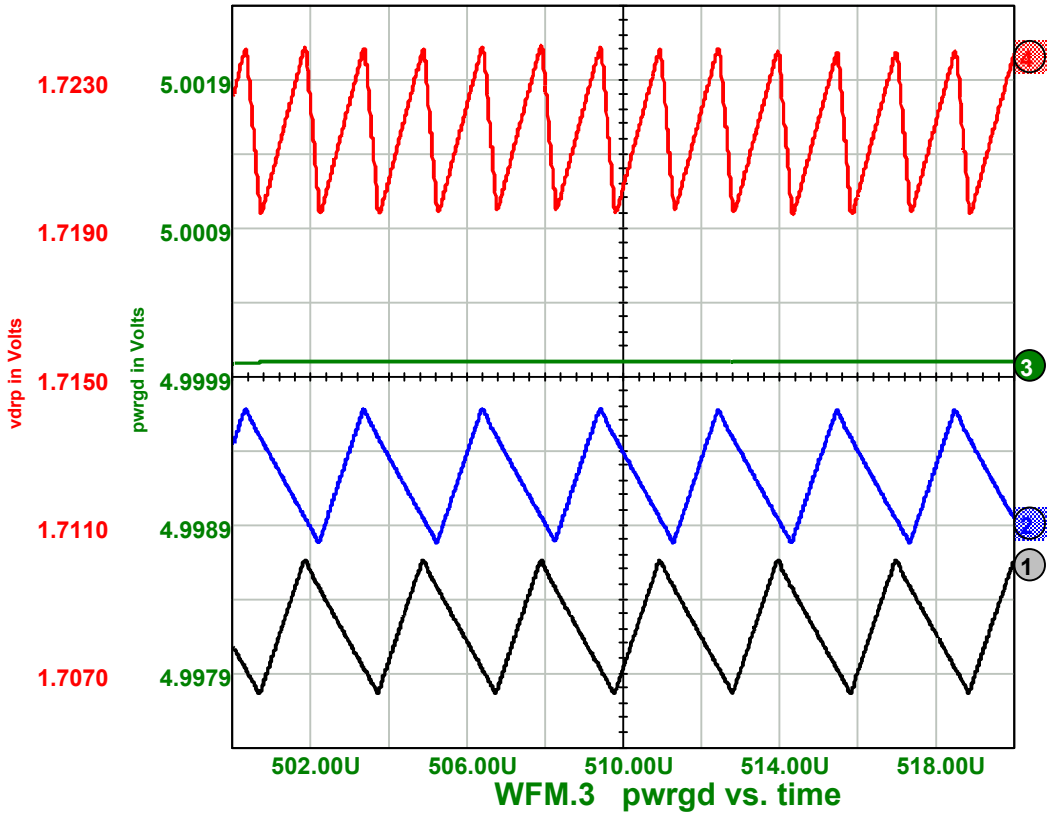

Figure 5.4.4 Spice Application Output Waveforms

Top to bottom: VDRP, PWRGD, CS2-CSREF, CS1-CSREF

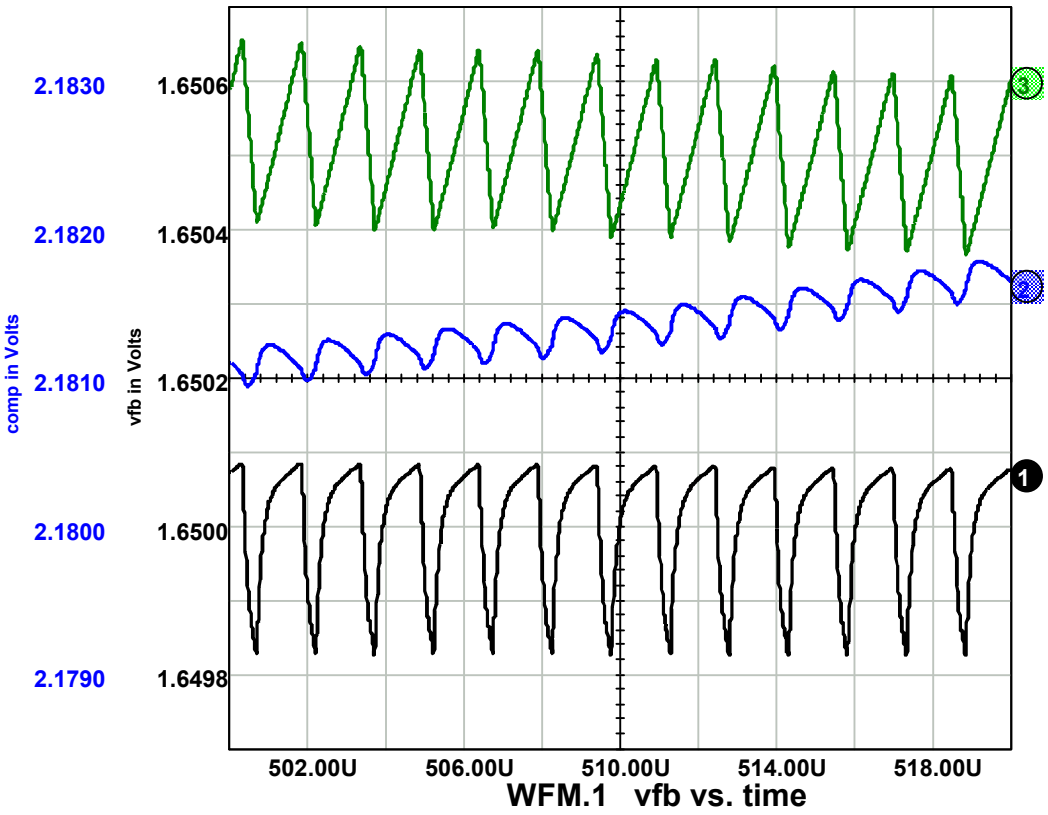

Figure 5.4.5 Spice Application Output Waveforms

Top to bottom: VOUT, COMP, VFB

5.5 Application Test Summary Table

Test	Test Conditions	Result	Specification
Frequency	Rosc = 39.2kΩ	331.1kHz	
Oscillator Phase delay	From Gate(H)1 to Gate(H)2	180°	165° min - 195°max
Vout	DAC=01000	1.65Vdc	1.65Vdc typical
Power Good Fault delay	CSREF=VDAC-15% to VDAC+15% DAC=11101	70.4us	50us min – 100us max

6.0 Conclusions and Recommendations

The Spice simulation results are within the manufacturer's electrical specifications.