

CS51220 Feed Forward Voltage Mode PWM Controller

1 Scope

This document contains the SPICE model, application circuit, and model description for the ON Semiconductor CS51220 Feed Forward Voltage Mode PWM Controller.

The model is split into two major functional blocks, the Main block and the Comparators block.

The Main block contains the Oscillator with Programmable Synchronization, the Feed Forward circuit, PWM comparator, output drive, and UVL comparator with Vref generator and disable.

The Comparators block contains the current limit, soft start, under and over voltage limits plus the soft hiccup circuit.

The blocks are built up from the sections described in the Tables below, listing their position in the circuit hierarchy.

CS51220 Main block		
Function	Implementation	Hierarchy
Oscillator	Sub circuit	Top level
PWM comparator	Sub-circuit	Top level
Reset latch	Sub-circuit	Top level
NOR, OR gate	Sub-circuit	All levels
NAND, AND gate	Sub-circuit	All levels
External Sync		Oscillator
UVL, Disable & Vref		Top level

CS51220 Comparator block		
Function	Implementation	Hierarchy
Over current comparator		Top level
Soft hiccup circuit		Top level
Under voltage comparator		Top level
Over voltage comparator		Top level
NOR, OR gate	Sub-circuit	All levels
NAND, AND gate	Sub-circuit	All levels
Fault latch		Top level
Soft start circuit		Top level

2 Assumptions

Behaviour is based on typical values given in the specification sheet for operation at 25 °C.

The model contains set-reset latches which will initialise correctly if the supply is ramped up from zero at the start of simulation.

3 Functional Description

The CS51220 is well described by the data sheet Block diagram. The Oscillator can be synchronised above or below its free running frequency and also provides a Sync output.

The oscillator turns on the output drive, V_o , at the start of every charging cycle and resets it at the start of the ramp discharge. The PWM comparator and Overcurrent comparator may cause early reset of the output drive while a number of fault conditions may inhibit the output drive completely.

Feedforward compensation for change of input voltage is provided as part of the PWM comparator. Overcurrent protection is provided through the soft hiccup facility which, effectively, shuts down and restarts operation through the soft start circuit.

3.1 The Oscillator

The oscillator schematic is given in Figure 1. An external capacitor is attached at node Ct. The capacitor is held reset by transistor Q1 until V_{ref} is established. The capacitor charge/discharge current is determined by the current flow in source V1 applied through source GB3.

Gates X1 to X4 form a set reset latch with a set threshold of 0.9 volts and a reset threshold of 2 volts. Source EB1 gives 0.9 volts for the latch set and 2 volts during reset. With V1 set at 1.065 volts and R2 at 1.1K the charge/discharge currents are 0.165/1.1 and 0.935/1.1 mAmps.

Gates X7 and X8 form an edge detector on the sync input, SYNCI. When a positive edge is detected the oscillator latch is reset to start a discharge cycle. The Sync pulse also drives the peak detector formed by D1 and C4, the voltage from this is used in EB2 to modify the charge/discharge currents to slow the oscillator. This allows for synchronisation below the free run frequency.

The voltage controlled delayed sync output signal is generated by subtracting the control voltage, V_{sd} , from the ramp voltage on Ct and feeding the result to gate X6 which acts as a comparator. Transistor Q2 provides the appropriate output drive levels.

3.2 The PWM comparator

The PWM comparator schematic is shown in Figure 2.

The two inputs to the comparator are the FeedForward ramp and a modified form of the output level feedback signal.

The FeedForward ramp is generated by an external RC circuit. The capacitor from the FF terminal to ground is charged by a resistor from the input supply and reset by transistor Q2 driven from the V_o signal. The peak amplitude of this signal is limited to 1.3 volts by diodes D1 and D2.

The other signal to the comparator is the least of the external compare input minus 1.2 volts, the soft start input, or 1.3 volts. This computation is performed in the combination of GB1 and EB3 with diodes D3 and D4 providing the 1.3 volt limit.

3.3 The reset latch

The reset latch sub-circuit is shown in Figure 3.

This is a simple set-reset latch with the reset side expanded to include inputs from the PWM and over-current comparators. The reset inputs are dominant.

3.4 The gates

Two input AND, OR, NAND, and NOR gates are used within the model. These use simple conditional expressions for the logic and are parameterised for input threshold and output level. The parameterisation allows the gates to be used as comparators where appropriate.

3.5 UVL, Disable & Vref

The Main sub-circuit is shown in Figure 4 with the elements described above included as sub-circuits. Gate X10 provides the Under Voltage Lockout with hysteresis while X6 provides Vref when the Disable and Vcc inputs allow.

3.6 Comparator block

Figure 5 includes all the elements of the comparator block described below.

3.7 Overcurrent comparator

EB2 compares the Isense and Iset inputs with a 0.2 volt offset. The comparison output, OC, also drives a peak detector D2, C1 which, with gate X4, provides the 50 microsecond timer for the NOOC signal used in the hiccup delay circuit.

3.8 Soft hiccup circuit

Gates X5 and X7 form the set-reset latch at the core of the soft hiccup circuit. The latch is set for an overcurrent signal occurring while the soft start signal is above 2.9 volts. This condition is generated in EB7. The latch is reset when the soft start signal goes below 0.3 volts and the NOOC signal is present calculated in EB8.

During hiccup the foldback current source connected to the Iset terminal is active, GB9 performs this function.

3.9 Under voltage comparator

EB5 forms the under voltage comparator with voltage level hysteresis built into the expression.

3.10 Over voltage comparator

EB6 is the over voltage comparator with R12 providing the input current hysteresis on this input.

3.11 Fault latch

Gates X1 and X2 form the fault latch, over or under voltage and low Vref signals set the latch with the set condition being dominant. The latch is reset by the softstart signal going below 0.3 volts as sensed in EB4.

3.12 Soft start circuit

An external capacitor is attached to node SS, the soft start terminal. GB3 provides the charge/discharge currents to the SS node while D1 and V5 provide voltage limiting. The initial high rate discharge feature during overcurrent is provided by gate X9 which senses SS greater than 2.8 volts during hiccup.

4 Model listing

Please see the ON_Power.lib file for the source listing.

5 Model tests

Tests use the circuit of Figure 6.

5.1 *External sync input*

The plot in Figure 7 shows the start of a Sync input pulse train. The ramp rate is slowed by 25% while the SYNCI pulse resets the ramp to lock to the SYNCI rate.

5.2 *Sync output*

Figure 8 shows the change of SYNCO timing with change of control voltage Vsd.

5.3 *FeedForward*

The effect of input voltage Feedforward is shown in Figure 9. The COMP input is set at 2 volts, as the input voltage rises so does the rate of charge at the FF terminal causing the output to be reset earlier in the cycle.

5.4 *Hiccup*

Figure 10 shows the soft start circuit recycling following the sensing of an overcurrent condition.

5.5 *CS51220 Application circuit*

Figure 11 shows the CS51220 model in an application circuit taken from the data sheet. The power up waveform obtained from this circuit is shown in Figure 12. The SPICE netlist for the circuit is given in Appendix A.

6 Conclusions

The model provides effective modelling of the CS51220 including the external sync features and soft hiccup operation during overload.

Note: Some figures have been removed due to the proprietary nature of the information.

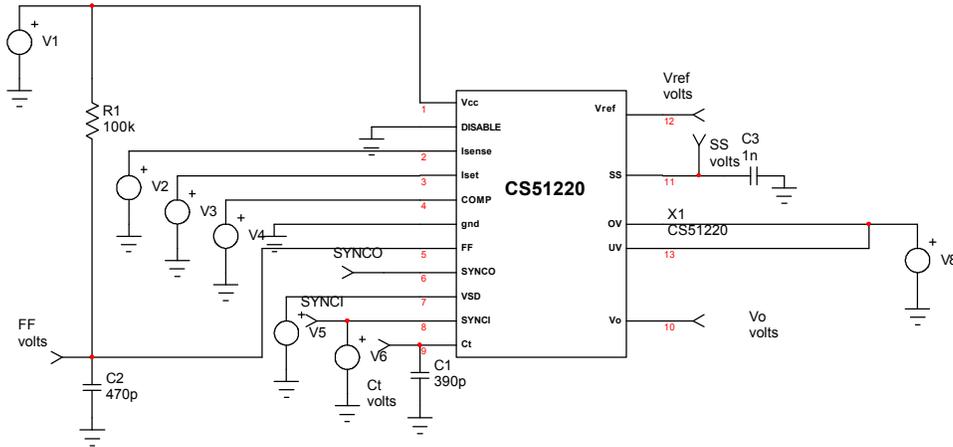


Figure 6 – Test circuit

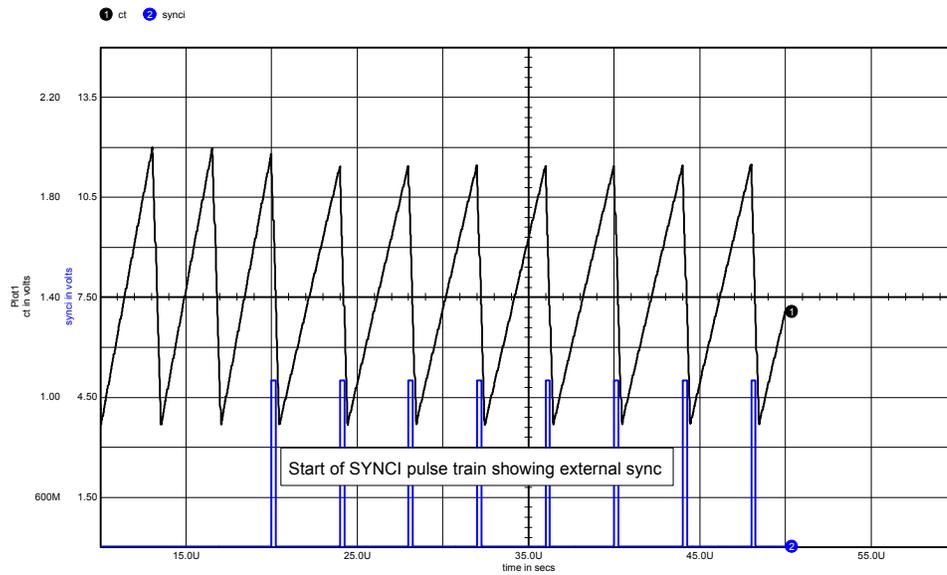


Figure 7 – External Sync

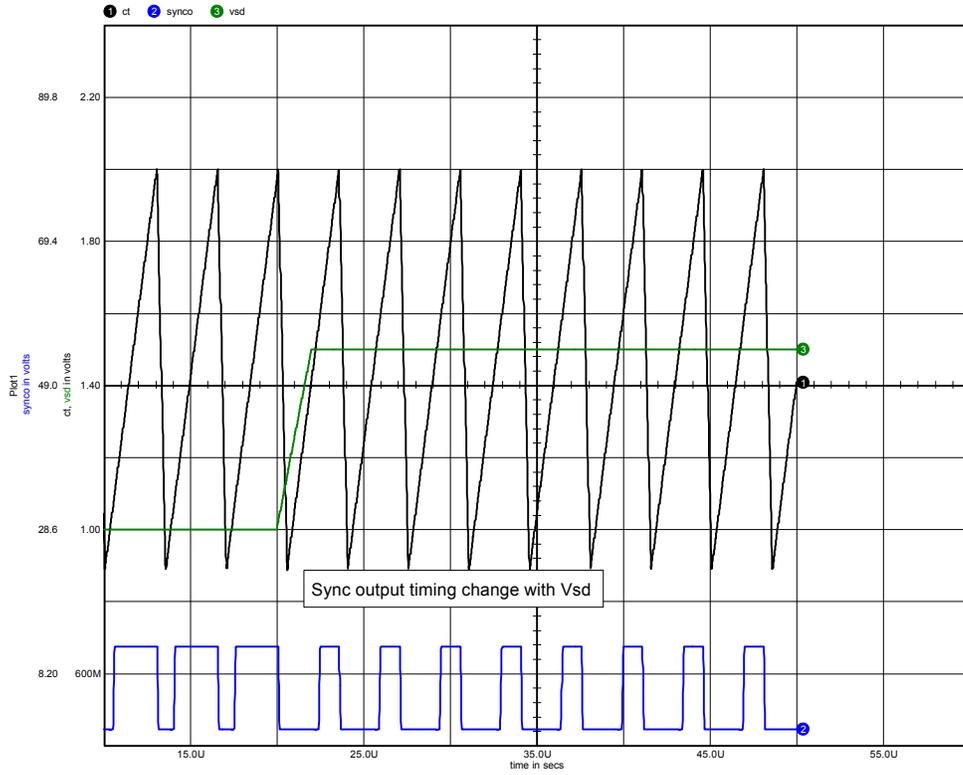


Figure 8 – SYNCO timing

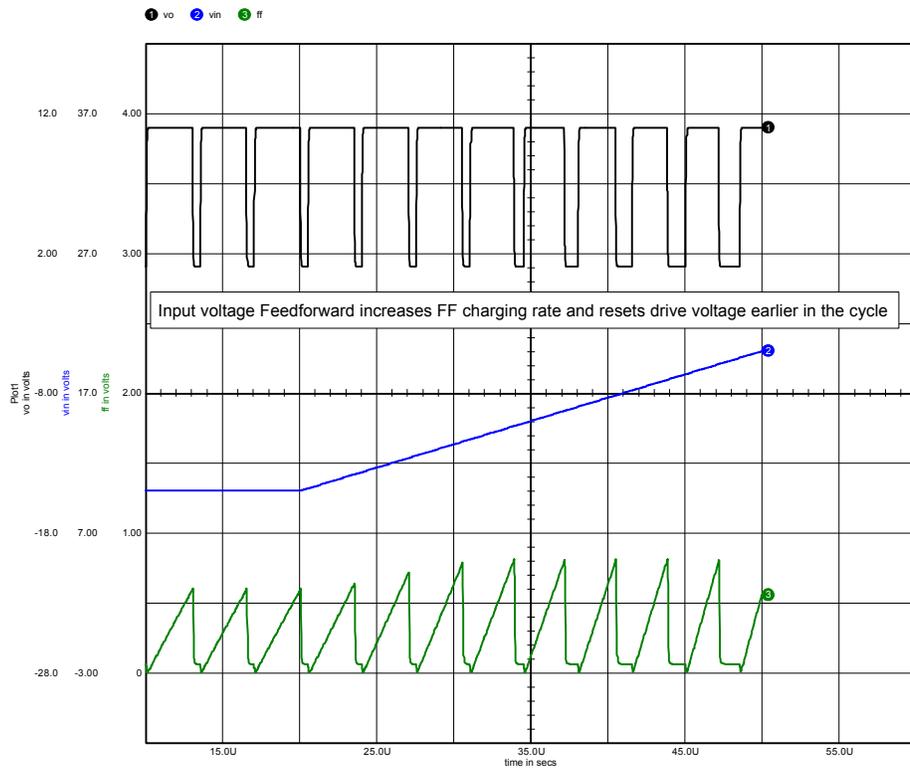


Figure 9 – Feedforward

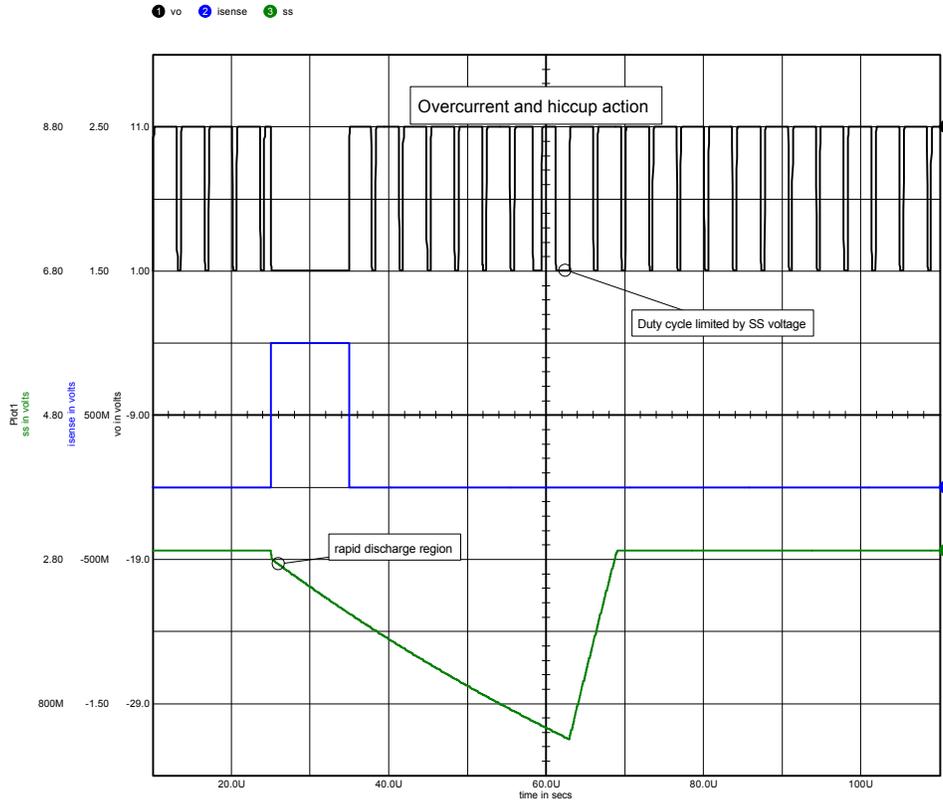


Figure 10 – Hiccup operation

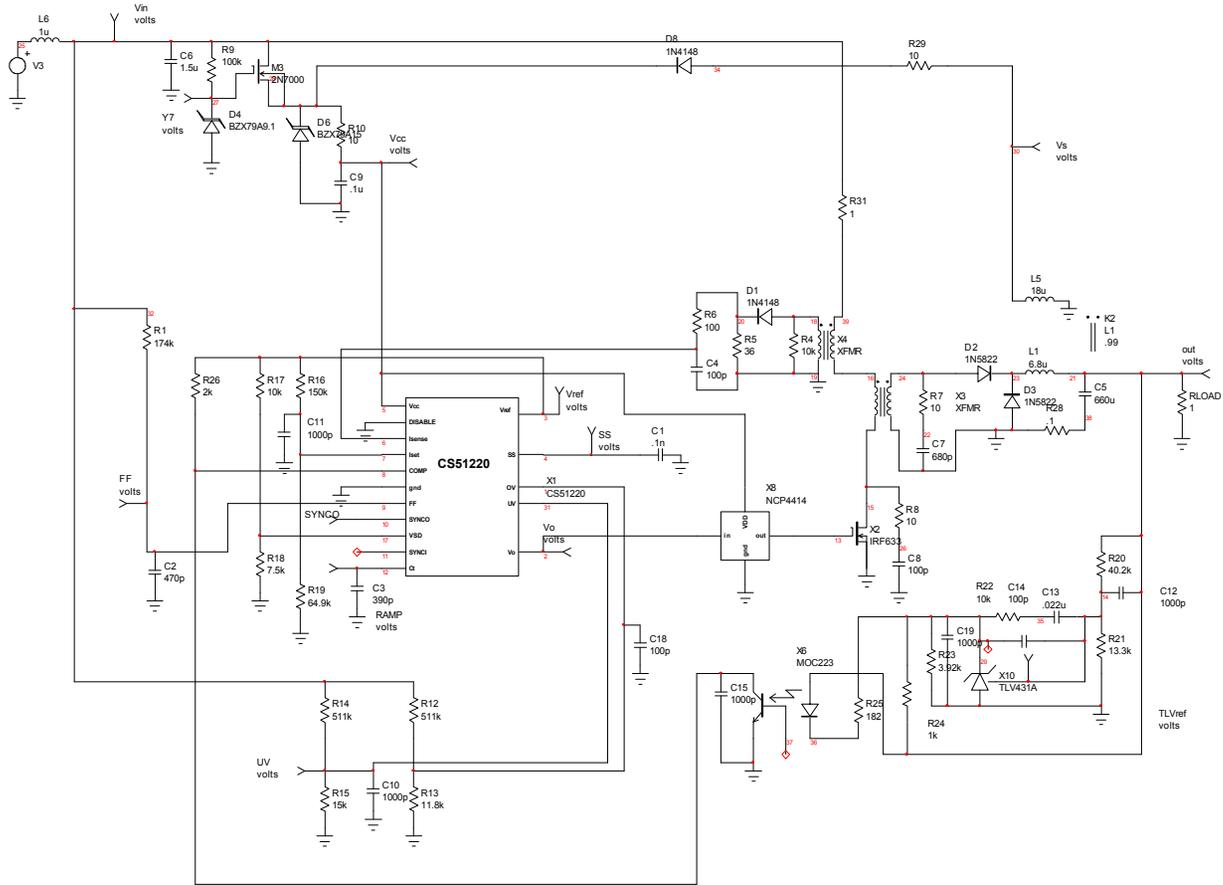


Figure 11 Application circuit

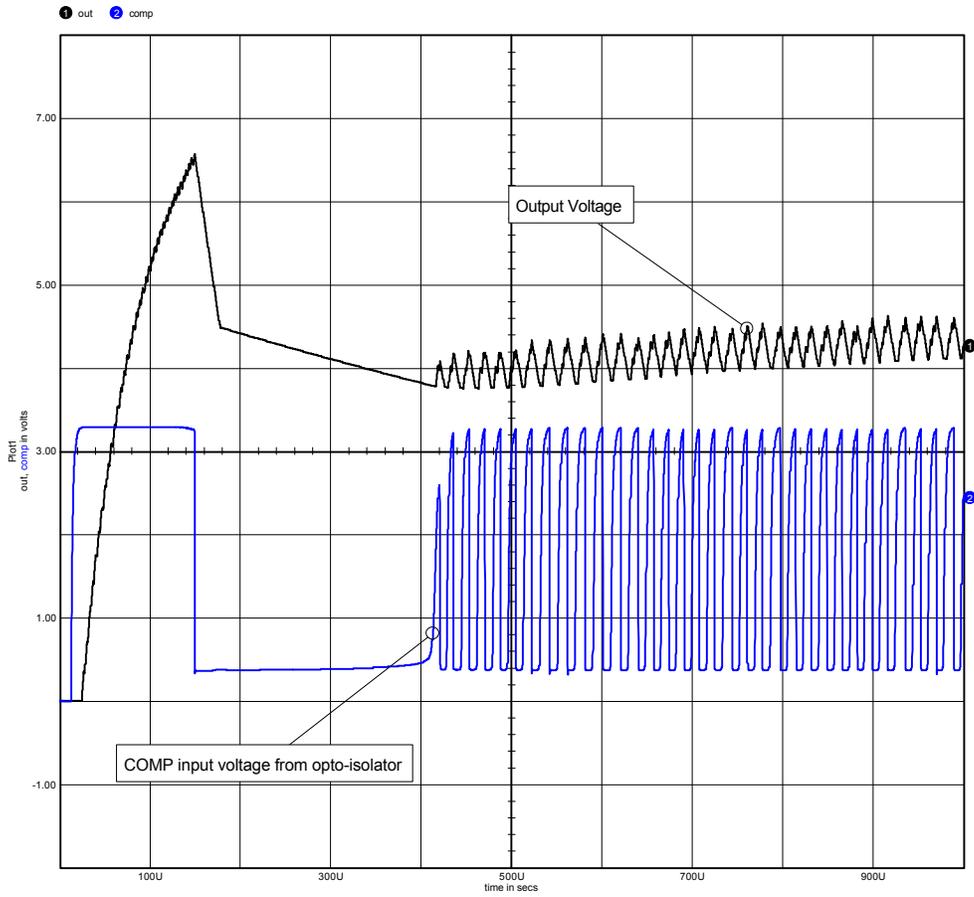


Figure 12 – Application circuit output and feedback waveforms