53111 90VDC – 0.8A solid State Relay

1.0 Scope

This document contains a description of the SPICE models and test and application circuits for the Micropac 53111 90V – 0.8A solid state relay.

Analysis:	**Solid State Relay**
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2.0 Functional Description

The 53111 is a SPST DC solid state relay (SSR). Functionally the device operates like a single-pole single-throw, normally open solid state relay. The SSR is actuated by an input current of 5 – 20mA. Output is provided by a power MOSFET exhibiting very low Rdson.

3.0 Model Description

The relay circuit was decomposed into elemental blocks, and then modeled accordingly as per the data sheet and specific topological IC information provided to AEi Systems by Micropac's engineers. Using PSpice, a model of the SSR was then created using the modules and a corresponding schematic and netlist was generated.

The model includes the following functionality and features:

- Proper transient response including variations with external components and capacitors across the outputs, from outputs to ground, from the inputs to ground, and across the inputs.
- Turn-on and turn-off vs. input current
- Proper connectivity as per the real-life part
- Turn-on and turn-off vs. temperature
- Rise and fall time
- Output On-Resistance
- Input forward voltage
- Input reverse breakdown
- Input & output capacitance
- Output transient rejection

- The input LED is modeled using D20. The DLED850N model provides the VI characteristics of the LED and will exhibit variations in operating point and temperature. The value of the SPICE model parameter N in the model is set to achieve the correct input forward voltage specification.
- The energy gap, EG, and the saturation current, IS, were adjusted to provide the correct VI response vs. temperature.
- The normal SPICE diode produces an increase in current flow with temperature. To generate a negative temperature coefficient response for the optical power, the arrangement of H1, R1, I2 and D11 were used.
- The nonlinear conversion response used in H2, EA1 and EB2 convert the optical power analog into the proper response for the photovoltaic diode stack current.
- EA1 is a table model that modifies the transfer response gain between the LED and photovoltaic diodes. At low drive currents a substantial gain factor is needed in order to get enough current to drive the photovoltaic diodes. At higher drive currents, much less gain is needed. The gain values were derived through

simulations in order to match Figure 4 in the data sheet (turn-on time vs. case temperature).

- Diodes D1-D19 (not including D11) represents the photovoltaic stacks.
- Other JFET and power Mosfet models were created using supplied data sheet parameters.

3.1 Assumptions

- Behavior is based on typical values given in the specification sheet for operation at 27 ºC.
- Some thermal variations are modeled and are represented in the subcircuit. However, in most cases sufficient data was not supplied in order to insure accuracy. The following aspects were attempted: LED V-I response, optical power vs. current, turn-off time, turn-on time.
- The SPICE syntax used is compatible with PSpice.

4.0 Model Verification

Initially a model for the input LED was developed. The model was tested using a simple circuit producing the VI curves that match the manufacturer's data sheet very closely. After that the value of the SPICE model parameter N was adjusted to provide the correct input forward voltage drop.

A test circuit corresponding to the switching waveform test circuit for the 53111 was then created, and shown in figures 4.1. The model was tested as per the manufacturer's datasheet using various values of drive current (5 – 20ma) and at different temperatures.

The results of the simulation performance for various model aspects are shown in figures 4.2-4.4.

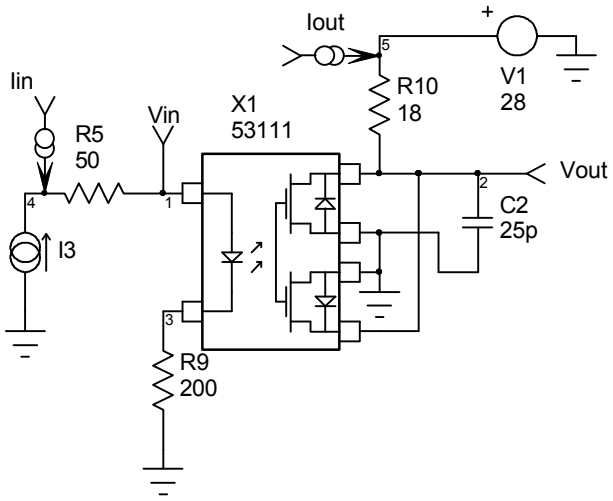

Figure 4.1: SPICE schematic diagram of the 53111 switching test circuit (DC Connection Configuration B).

Both A (AC/DC connection) and B (DC connection) configurations were tested and found to produce the correct output on-resistance and output voltage levels

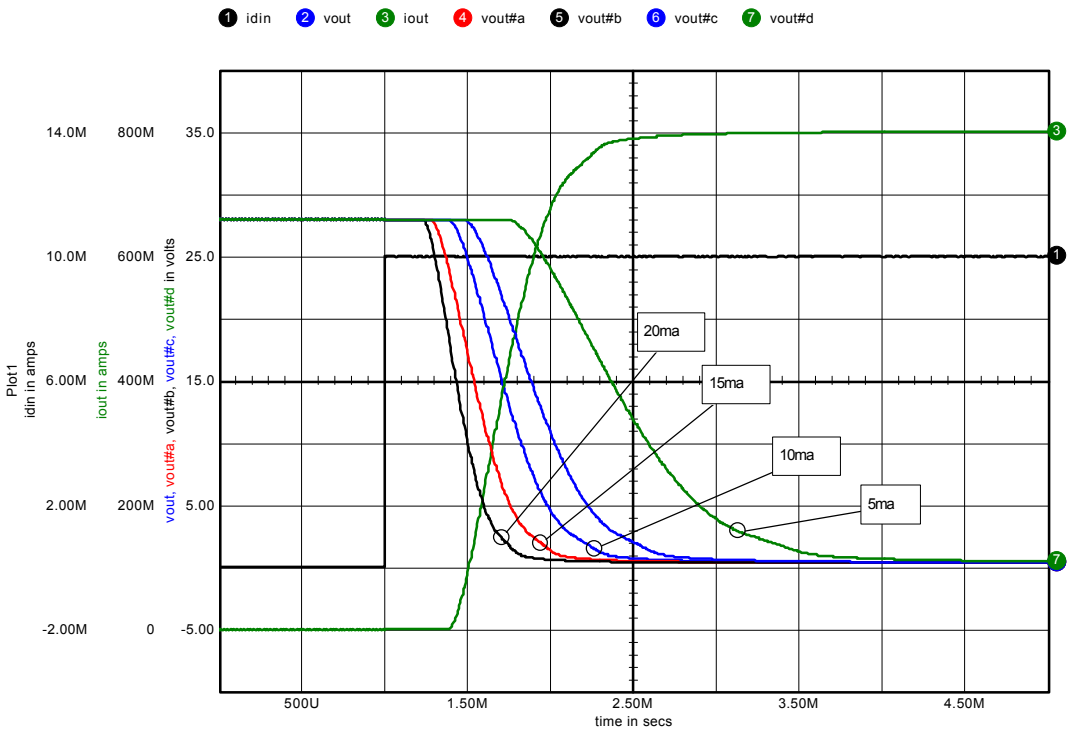

Figure 4.2: T-on Simulation results showing the input current pulse (10ma peak wfm 1), and output voltages (VOUT) for several different drive currents.

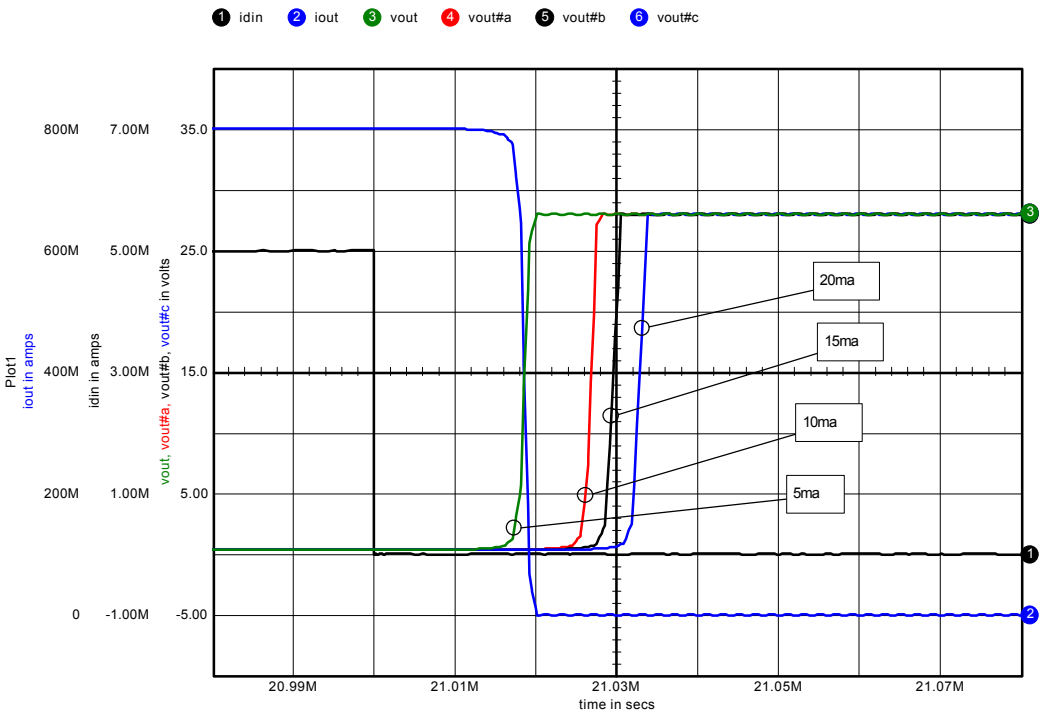

Figure 4.3: T-off Simulation results showing the input current pulse (10ma peak wfm 1) and output voltages (VOUT) for several different drive currents.

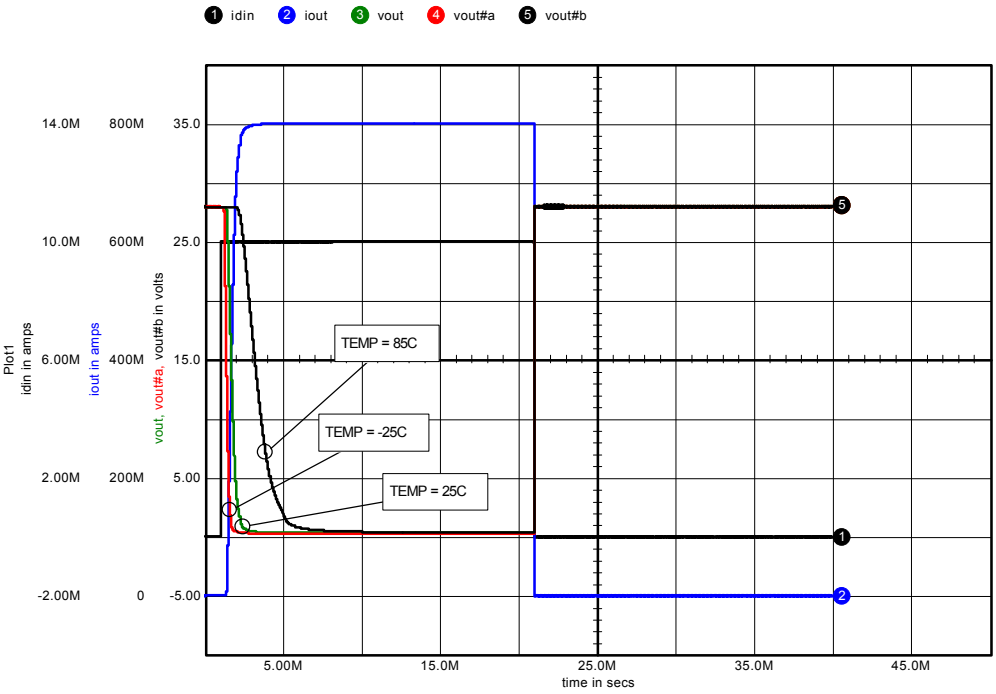

Figure 4.4 Turn-on and turn-off times vs. temperature.

Figure 4.5 shows the output transient test circuit. V1 uses a 50V pulse. The VM output pulse peak to peak value is 3.42V which is less than the 10% of VO(peak) specification.

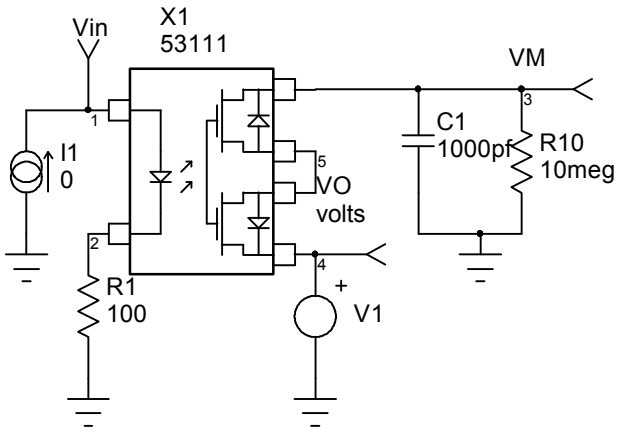

Figure 4.5 Output Transient rejection test circuit.

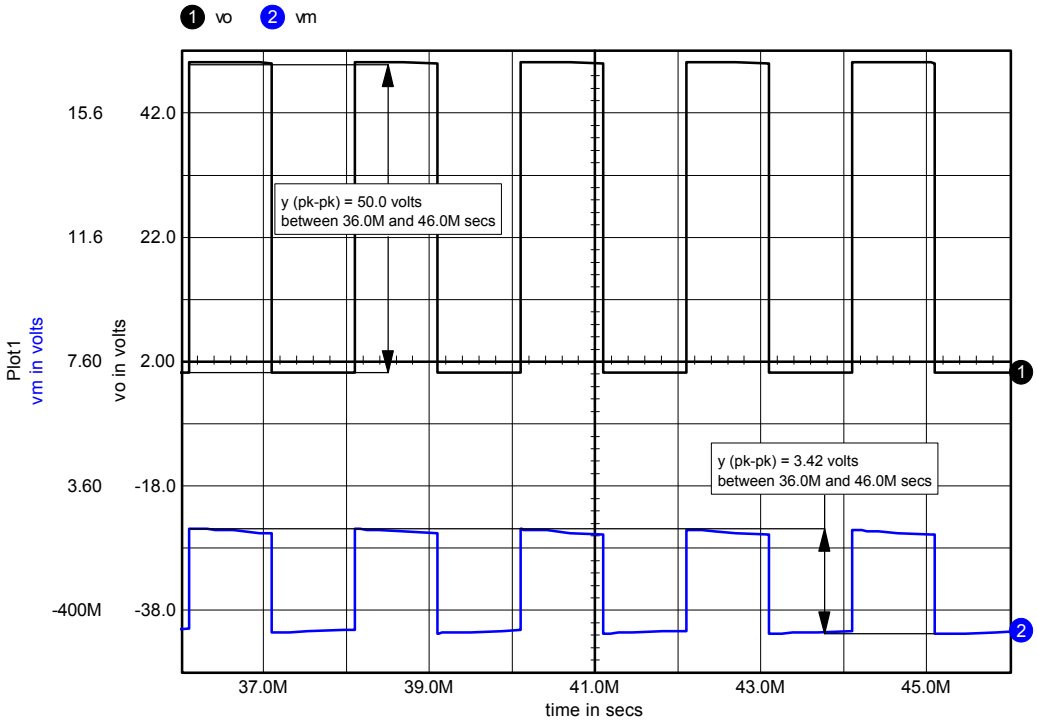

Figure 4.6 Output Transient rejection test results. VM is less than the 10% of VO(peak) value.

5.0 Conclusions

The model of the 53111 90V –0.8A solid state relay correlates very well with the manufacturer's datasheet. This data should be verified against actual hardware for further confirmation.