

An Improved SPICE Capacitor Model

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In the world of power conversion, not all capacitors are created equal. In many circuits the characteristics of the capacitors dominate the performance of the circuit.

SPICE simulators include a capacitor primitive element. The primitive element does not include parasitic elements, such as series resistance or series inductance. In many cases these are negligible and in other cases they can be easily added to the circuit model as separate elements. This is complicated by the fact that the resistance, capacitance and inductance are frequency and temperature dependent. The purpose of this paper is to investigate the impact that the capacitor characteristics can have on circuit performance and to develop a simple capacitor subcircuit which allows an improvement in simulation accuracy, without requiring a great deal of time to develop the model.

A military style CLR79 capacitor was measured for impedance and phase using a Hewlett Packard Impedance Analyzer. The results of the measurement are shown in figure 1. The new subcircuit was used to simulate the capacitor. The results of the simulation are shown in figure 2.

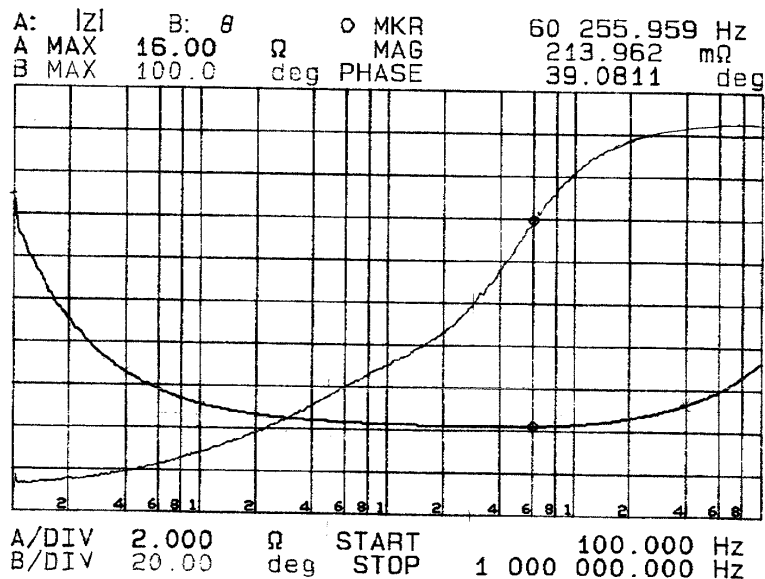


Figure 1 Measured Impedance - 160 uF CLR79 Capacitor

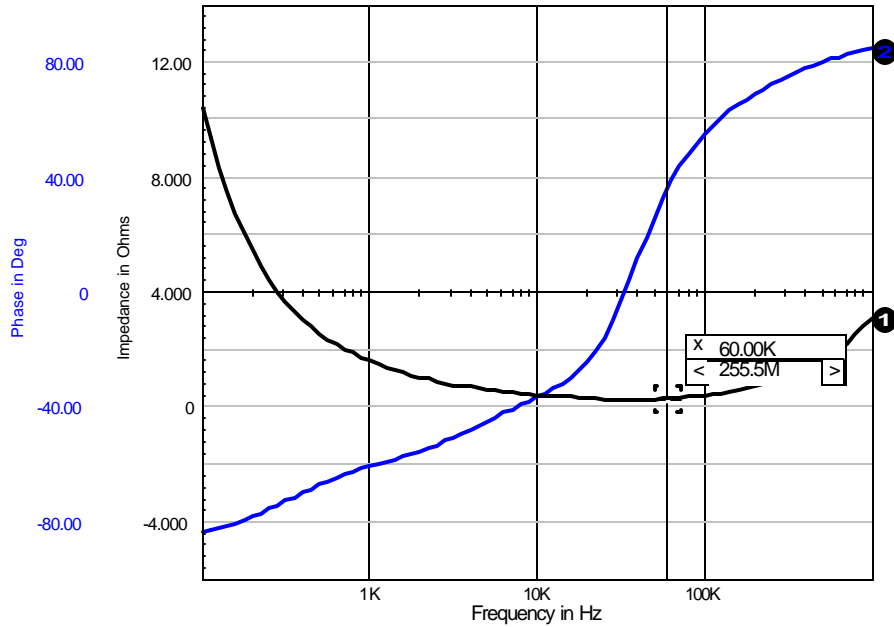


Figure 2 Simulated Impedance - 160 uFd CLR79 Capacitor

The correlation between the simulated and measured results are excellent. The subcircuit representation is used as the basis of comparison for the remainder of this paper.

For comparison to the actual capacitor impedance, a simple representation using an external series resistance and inductance was created. The SPICE schematic representation of this circuit is shown in figure 3.

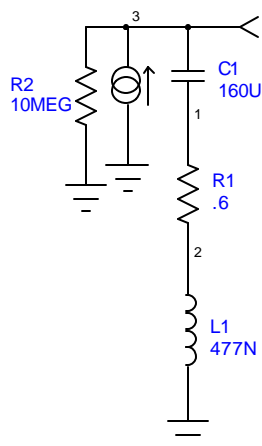


Figure 3 SPICE Representation of Capacitor

This model is consistent with our diligent efforts, as engineers, to include all parasitics in our SPICE models (Uh Huh). The results of this simulation are shown in figure 4 and figure 5. Figure 4 shows the impedance of the circuit shown in figure 3 and the error between figure 3 and the new subcircuit. Figure 5 shows the phase of the circuit in figure 3 and the error between figure 3 and the new subcircuit.

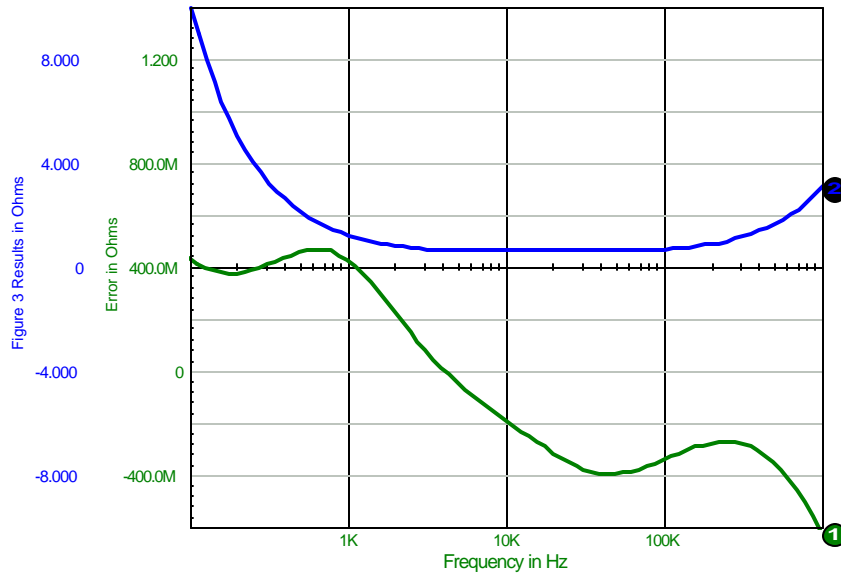


Figure 4 Figure 3 Results and ESR Error

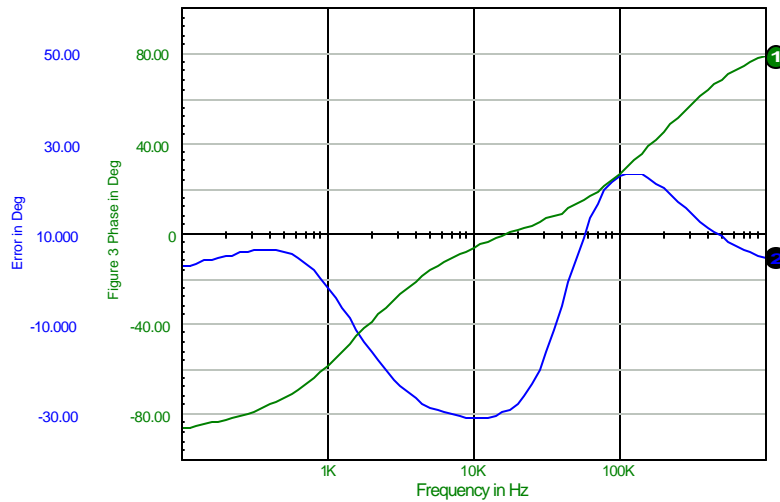


Figure 5 Figure 3 Results and Phase Error

The results indicate a reasonable average error. The average impedance error is only 45 milliohms and the average phase error is 3 degrees. The RMS error is considerably worse, the RMS impedance error is 345 milliohms and the RMS phase error is 17.8 degrees. The maximum errors are 620 milliohms impedance and 31 degrees phase. Even worse is the location of the errors. The impedance errors are maximum at approximately 700 Hz and 50 kHz. These are near the normal switching frequency for switching power supplies and near the resonant frequency of many output filters. The phase errors are maximum in the range of 5 kHz to 20 kHz and at 100 kHz, again near the switching frequency of many switching power supplies.

These errors can easily skew the phase margin and gain margin results of power supply simulations as well as creating large errors in the output ripple simulations. A simple example circuit is used to illustrate the effects of these errors. This simplified model is shown in figure 6.

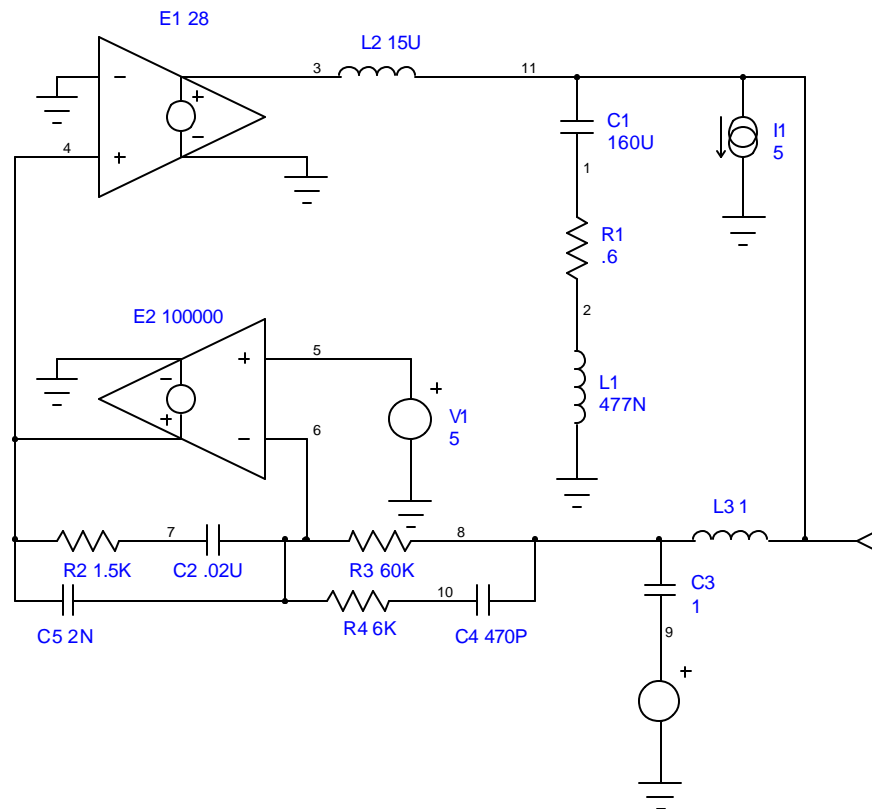


Figure 6 Simplified Power Converter SPICE Model

The SPICE model, shown in figure 5 was simulated to measure the open loop phase and gain in order to measure the bandwidth and the phase margin. The results of the simulation are shown in figure 7. The same circuit was simulated with the new capacitor subcircuit in place of the simplified representation. The results of this simulation are shown in figure 8. For comparison a primitive capacitor (without ESR and ESL) was simulated. The results are shown in figure 9.

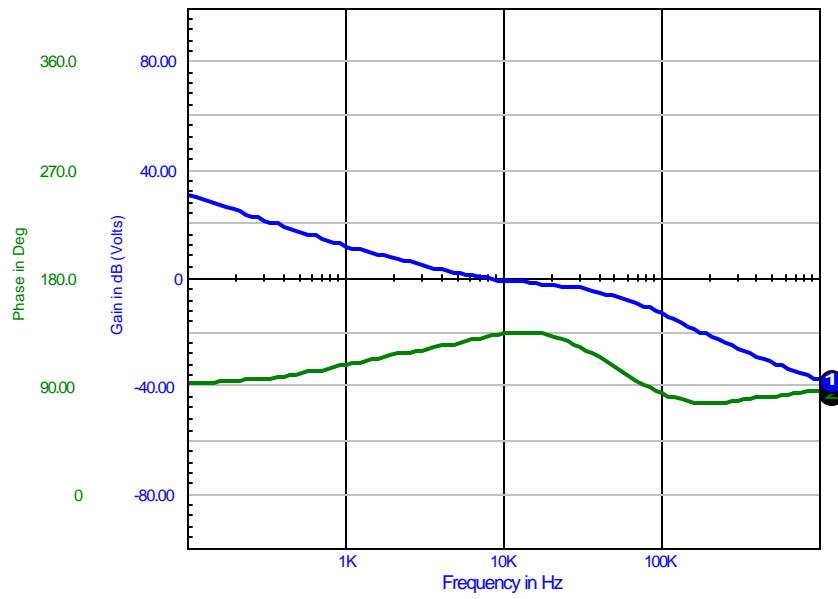


Figure 7 Open Loop Gain and Phase with Simplified Capacitor

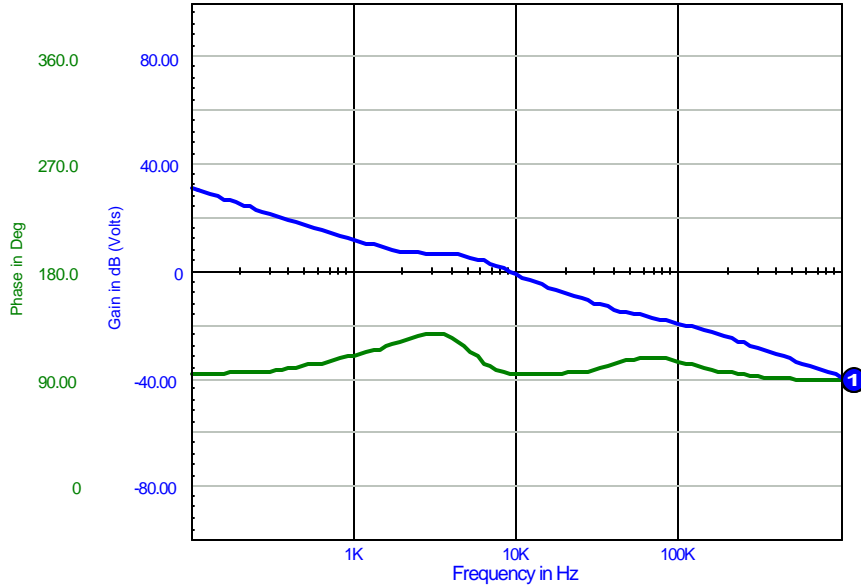


Figure 8 Open Loop Gain and Phase with new Cap Subcircuit

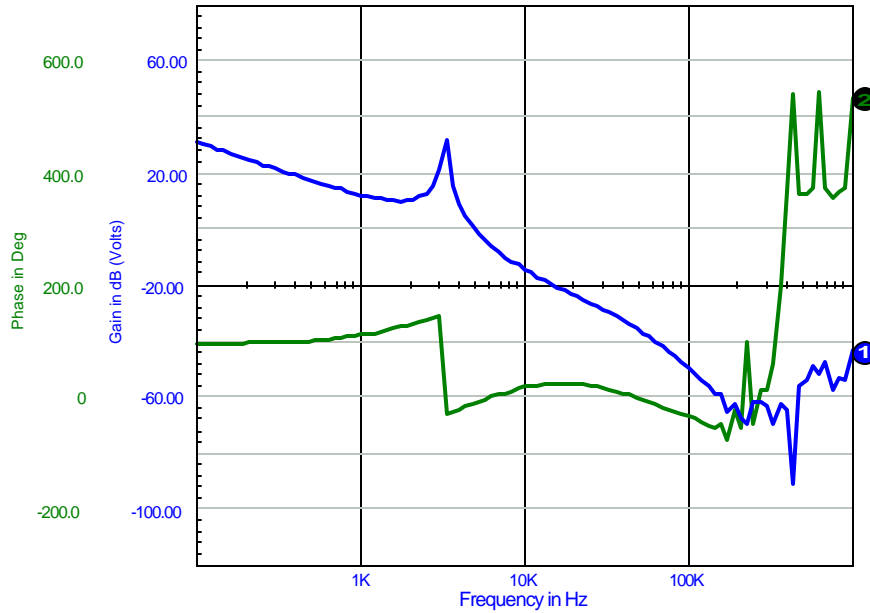


Figure 9 Open Loop Gain and Phase with Primitive Capacitor

The results of these three simulations are summarized in table 1 below

Table 1 - Open Loop Gain and Phase Results

	Simplified Model	New Subcircuit Model	Pure Capacitor
Phase Margin	129.7 degrees	93.9 degrees	-13 degrees
Bandwidth	7.18 kHz	8.65 kHz	4.88 kHz

The three simulations show the vastly different results which can be obtained simply by modifying the accuracy of the output capacitor model. It is important to note that the results of the pure capacitor model are unstable and could be representative of actual results obtained with very high quality output capacitors, such as ceramic.

The effects of the capacitor model on the output ripple are also investigated using a greatly simplified SPICE model of a switching power supply. The SPICE schematic for this model shows the output filter of a switching power supply driven by a simple pulsed voltage source. The results of the output ripple voltage are simulated. The SPICE schematic for this simulation is shown in figure 10. The results of the simulation are shown in figure 11 and figure 12. The results with the simplified capacitor model are 2.4 volts peak-peak while the ripple with the new capacitor subcircuit is only 1.4 volts peak-peak.

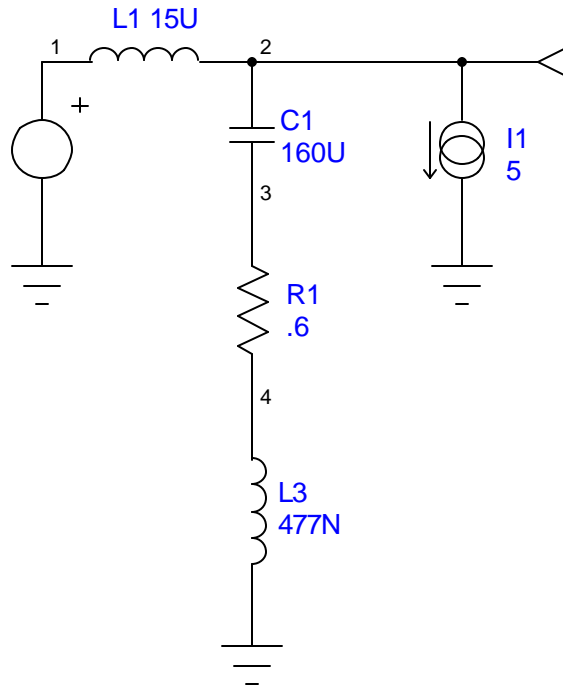


Figure 10 Output Ripple SPICE Schematic

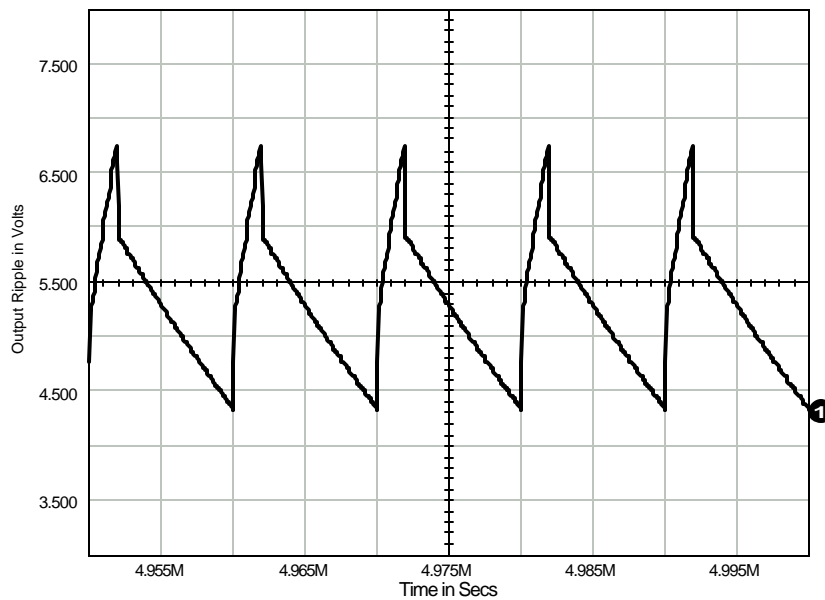


Figure 11 Output Ripple Simplified Capacitor

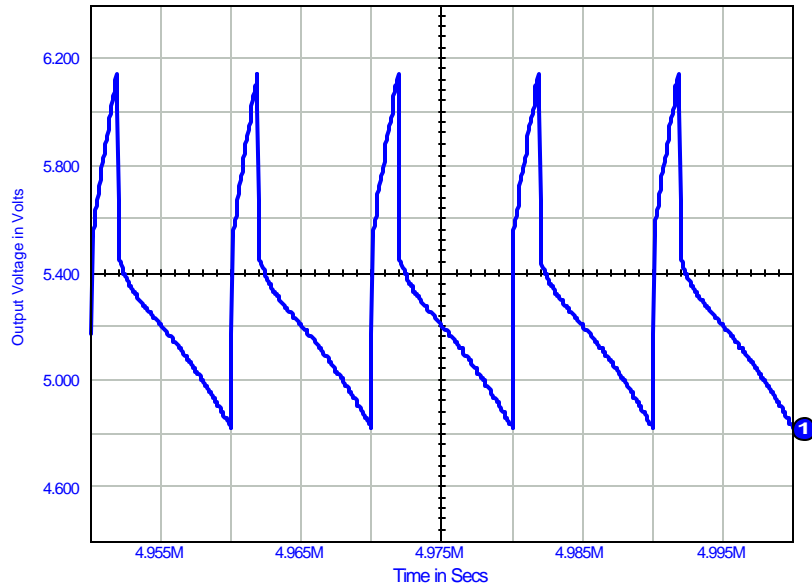


Figure 12 Output Ripple New Subcircuit

The SPICE schematic for the new capacitor subcircuit model is shown in figure 13. The subcircuit is based on a simple capacitor ladder network. This technique was described by Intusoft in Issue #45, dated Feb. 1996, of their newsletter.

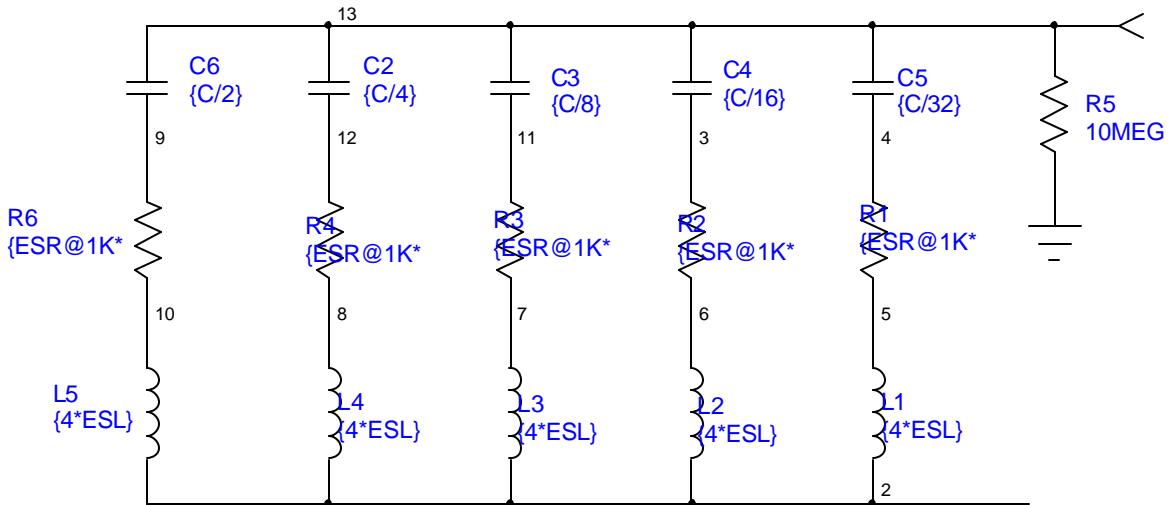


Figure 13 SPICE Schematic of New Capacitor Subcircuit

The SPICE netlist for the new capacitor subcircuit is listed in Table 2.

Table 2 New Capacitor Subcircuit

```
.subckt clr 13 2
C3 13 11 {C/8}
C4 13 3 {C/16}
C5 13 4 {C/32}
R1 4 5 {ESR@1K*1.25}
R2 3 6 {ESR@1K*0.9}
R3 11 7 {ESR@1K*1.75}
R4 12 8 {ESR@1K*2.32}
C6 13 9 {C/2}
R5 13 0 10MEG
R6 9 10 {ESR@1K*6.25}
L1 5 2 {4*ESL}
L2 6 2 {4*ESL}
L3 7 2 {4*ESL}
L4 8 2 {4*ESL}
L5 10 2 {4*ESL}
R8 2 0 10meg
C2 13 12 {C/4}
.ENDS
```

Two additional capacitors were measured and simulated to further verify correlation. The results are shown in figures 14 through figure 17. The SPICE netlist for the impedance simulations are shown in table 3.

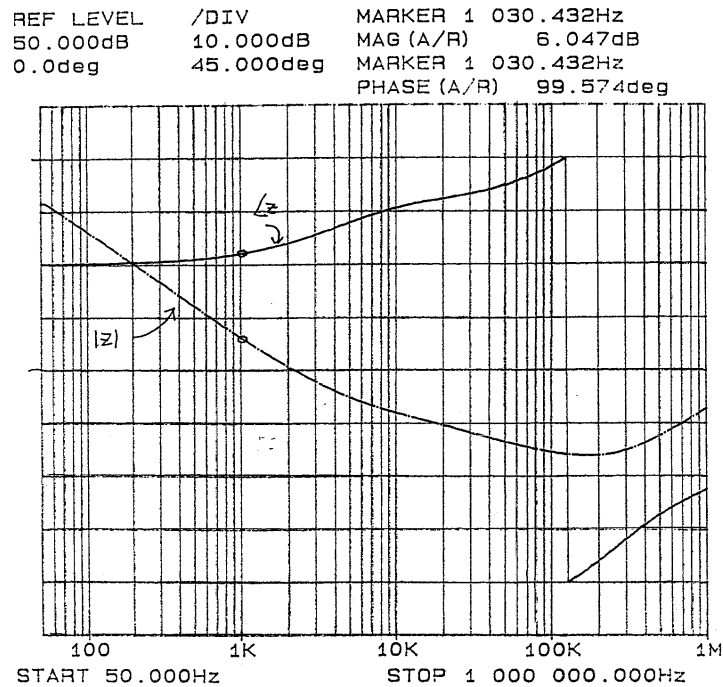


Figure 14 Measured Impedance - 86 uF CL79 Capacitor

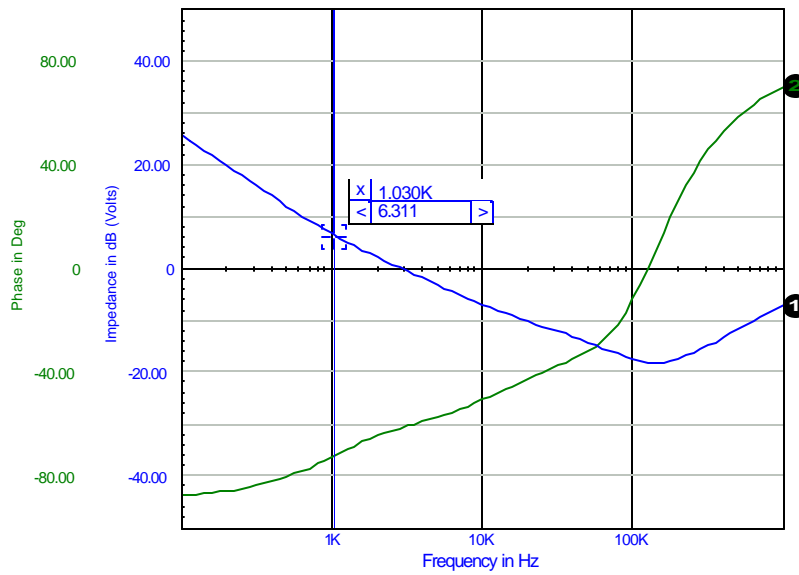


Figure 15 Measured Impedance - 86 uFd CLR79 Capacitor

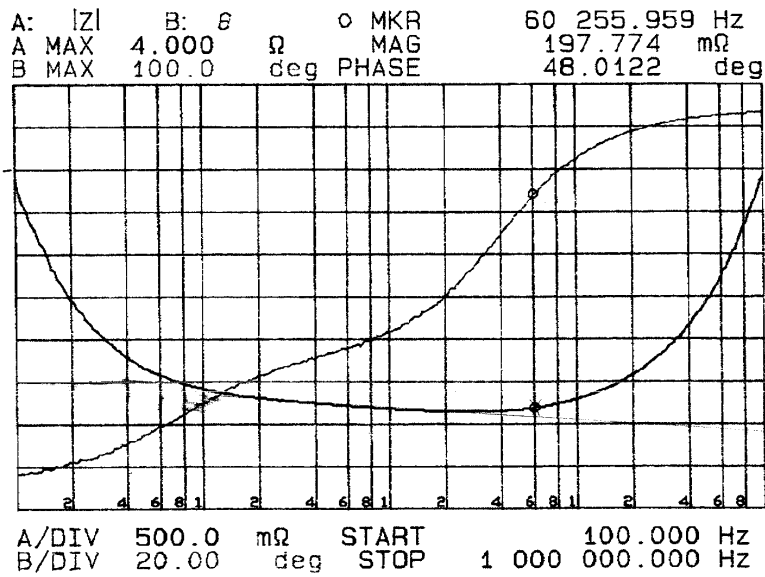


Figure 16 Measured Impedance - 540 uFd CLR79 Capacitor

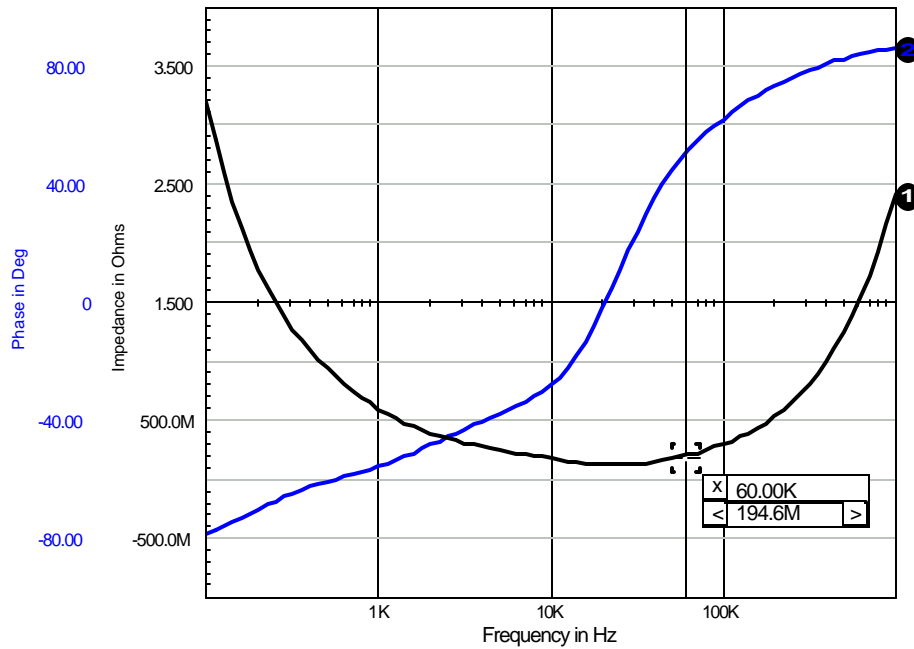


Figure 17 Simulated Impedance - 540 uFd CLR79 Capacitor

Table 3 SPICE Netlists to Simulate Capacitor Impedance

```
F:\S_BAND\captest
*SPICE_NET
*INCLUDE NEW.LIB
.AC DEC 20 100 1MEG
.PRINT AC V(1) VP(1)
II 0 1 AC 1
X1 1 0 CLR {C=160U ESR@1K=.6 ESL=477N }
.END
F:\S_BAND\captest
*SPICE_NET
*INCLUDE NEW.LIB
.AC DEC 20 100 1MEG
.PRINT AC V(1) VP(1)
II 0 1 AC 1
X1 1 0 CLR {C=86U ESR@1K=.35 ESL=80N }
.END
F:\S_BAND\captest
*SPICE_NET
*INCLUDE NEW.LIB
```

```
.AC DEC 20 100 1MEG  
.PRINT AC V(1) VP(1)  
I1 0 1 AC 1  
X1 1 0 CLR {C=540U ESR@1K=.35 ESL=477N }  
.END
```

It is important to understand the effects and importance that a simple effect, such as capacitor parasitic elements can have on circuit performance and simulation results. The old saying “garbage in - garbage out” still applies. In addition all capacitors are not created equal. I hope that this simple subcircuit will help to separate fact from fiction, and may also find itself as a useful tool in the selection of capacitors for switching power supply designs.

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