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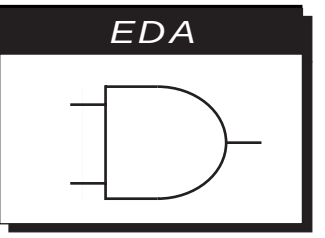

Spice helps analyze, optimize regulator stability

Steven M Sandler

Last month's column introduced some stability issues associated with a popular regulator IC, the LM317 and its variants. It outlined why these problems arise and discussed possible means of measuring the problem, complete with the test circuit's Spice listing. This column continues the discussion by examining how to simulate, predict and optimize stability.

Predicting stability

Even though predicting regulator stability presents difficulties, software simulations can help. For instance, a Spice model of the circuit (Fig 1) provides a Bode response. The graphical results of the stability simulation with C_{adj} = 0 appears in Fig 2a. Note that the simulation uses 1 pF as a placeholder because Spice doesn't allow a zero-value cap. These simulation re-

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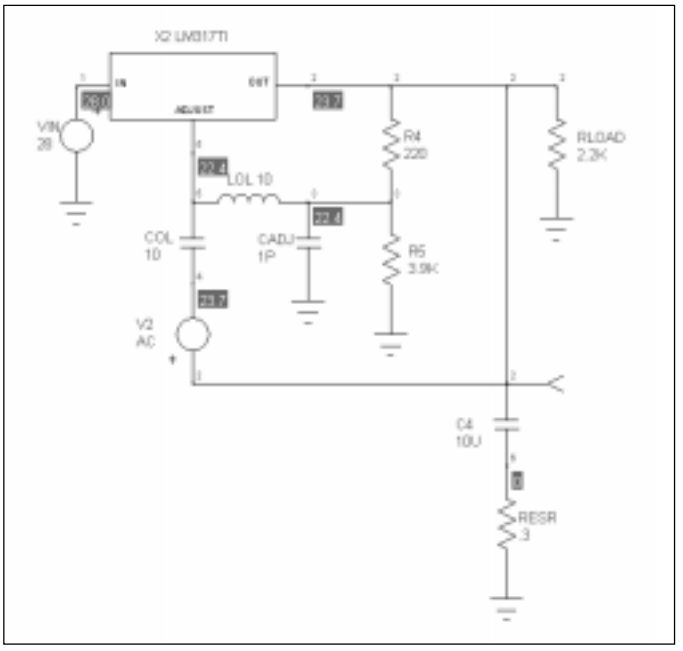

Fig 1—A Spice model of the test circuit to evaluate regulator stability uses 1 pF as a placeholder because Spice doesn't allow a zero-value capacitor.

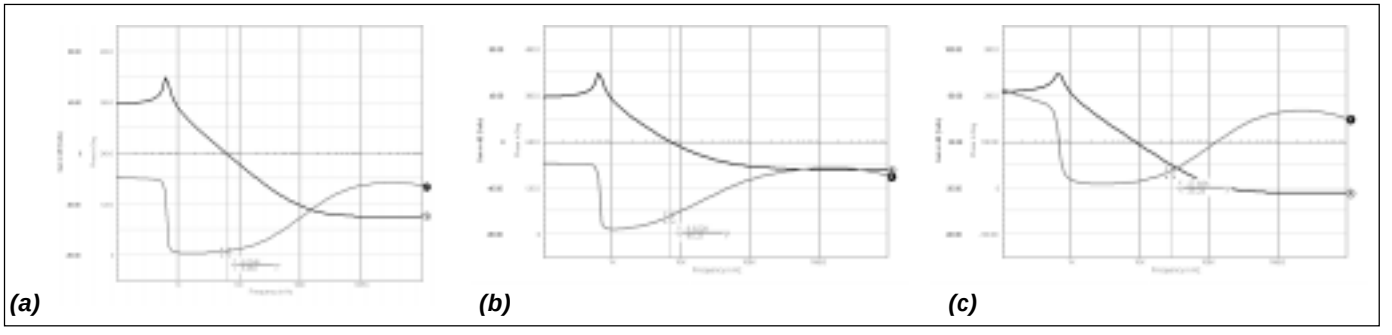

Fig 2—Spice simulations of the test circuit in Fig 1 with values of C_{adj} equal to 0 (a), 0.0047 μF (b) and 10 μF (c) give results close to those measured in an actual circuit.

sults match results of the network-analyzer-based test circuit presented last month, and the software approach allows faster and easier tests with different combinations of parts as opposed to the physical world.

The author repeated simulations with an adjustment capacitance of 0.0047 µF (Fig 2b) and 10 µF (Fig 2c). In all three cases the simulation results are very close to the measured results. However, the Spice results reflect a slightly higher bandwidth than the measurements. If you reduce the simulation gain results by approximately 15% to match the measured bandwidth, the resulting phase margin is much closer, as indicated in brackets in the comparison of Table 1. It's worth noting that 15% is probably well within the component tolerance of the LM317 bandwidth.

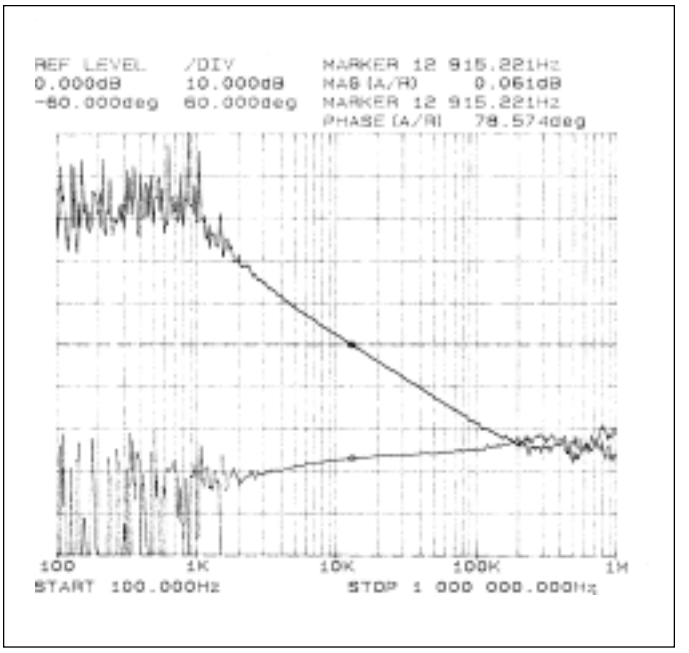

Fig 4—To verify the simulation, the author ran a test setup using a network analyzer with a 0.082-µF cap, and you can see the phase margin of 79°.

Optimizing it

With the problem clear and a valid Spice model to represent the circuit, optimizing the circuit presents no great challenge. One method uses Spice's Optimizer function, or Sweep function, to incrementally increase the value of the adjustment capacitor while measuring phase margin for each value of capacitor. The ICAPS/4 Spice-compatible file for the optimizer simulation appears in Listing 1. The resulting graph (Fig 3) indicates that the phase margin vs C_{adj} is parabolic and the optimum value is near 0.082 µF.

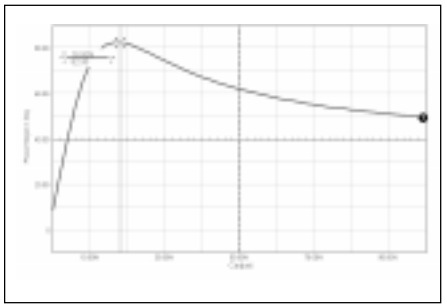

Fig 3—Running the Spice deck in Listing 1 for the optimizer simulation that varies the adjustment capacitor generates the above plot and shows an optimum value near 0.082 µF.

To check the simulation results, the author ran the test circuit with the network analyzer with an 0.082-µF cap and got the results in Fig 4. The 79° phase margin is very close to the expected 82°. Increasing the adjustment capacitor to 0.028 µF reduces phase margin to 73°. This value is again close to the simulated value, and it also confirms that further increases in capacitance further decrease the phase margin, lending credibility to the optimized solution.

Readers who don't have Spice or even a network analyzer can still find an approximation of an optimum solution. Using step load data, go to the minimum operating current and measure the ringing frequency. If no ring-

		Spice Results		Measured Results	
R Load	C adj	Phase Margin	Bandwidth	Phase Margin	Bandwidth
2.2 kΩ	0	8.5°	6.05 kHz	8.8°	5.26 kHz
2.2 kΩ	0.0047 µF	45.2°	6.82 kHz	38.5°	5.79 kHz
2.2 kΩ	10 µF	35.2°	27.68 kHz	28.1°	24.6 kHz

Table 1—A comparison of a software simulation with actual tests for varying values of C_{adj} shows that phase and bandwidth have very close values.

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Listing 1--Test circuit simulation

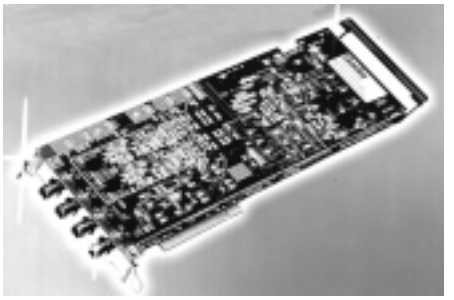
```
*SPICE_NET
*INCLUDE REG.LIB
.OP
.AC DEC 20 100 10MEG
.PRINT AC VDB(2,3) VP(2,3)
*.TRAN .1U 1000U 0 1U
.OPTIONS METHOD=GEAR ITL4=1000
GMIN=1N ABSTOL=1U
*OPT CADJ=1P TO 100N STEP=2N
.PRINT TRAN  V(2)
LOL 5 3 10
R4 2 3 220
R5 3 0 3.9K
VIN 1 0 28
COL 5 4 10
V2 2 4 AC 1
C5 3 0 CADJ
C4 2 6 10U
RLOAD 2 0 2.2K
RESR 6 0 .3
X2 1 5 2 LM317TI
.END
```

ing is present, you're done. If ringing is present, its frequency gives the regulator's approximate bandwidth. Then the relationship $C_{adj} = 1 / (\pi \cdot Freq \cdot R2)$ selects the adjustment capacitor. A cap of this value puts a zero in the control function one octave before the regulator's lowest bandwidth. In the test circuit, the minimum ringing frequency is approximately 5 kHz and the value of R2 is 3.9 kΩ. The approximate solution for the cap is then 0.016 μF, which is very close to the optimum solution. ***PE&IN***

Editorial Feedback
This article's value to me was:
High—272 Average—273 Low—274

NEW PRODUCTS

High-speed data acq



Capable of digitizing one channel at 100M samples/sec with 12-bit resolution (or sampling its two channels at 50 MHz each), the CompuScope 12100 costs $5995. Its dual A/Ds operate in a ping-pong fashion, and on-board autocalibration circuitry matches the two to reduce image signals. The bus-mastering PCI card transfers data from its onboard memory—from 1M to 4M samples—to host memory at rates to 100M bytes/sec. The two inputs accept signals in full-scale ranges from ±100 mV to ±5V with either ac or dc coupling and spec a bandwidth of 40 MHz. Purchasers get a copy of GageScope for DOS, while GageScope for Windows is optional; drivers for DOS, Win95/NT sell for $250 each. ***Gage Applied Sciences Inc*** (S Burlington, VT (800) 567-4243). ***Circle VIP No 106***

Motion controller

Operable either standalone or under PC control, the ACR2000 features a 27-MHz TMS20C3X and an onboard preemptive multitasking realtime OS. The AT-bus card handles two ($1600) or four ($1875) axes of motion, either steppers or servos in pairs. It generates 16-bit servo signals in the range ±10V dc and for steppers specs a velocity range to 4 MHz and pulse-width range from 125 nsec to 16 μsec. The kernel can handle a number of tasks simultaneously: perform eight motion programs with 50-μsec/axis servo update rates; perform eight other non-motion programs; command eight PLC programs with a 2- to 5-msec scan time; command four comm ports (two serial ports, the ISA bus and a parallel port). All ports can operate simultaneously and attach to different programs, and some programs can run while you're editing others. Users access the card's controller firmware in AcroBasic with either manual-data input or by executing commands from a stored program. Other hardware features include 32 optically isolated digital I/O lines that handle 24V dc, two 64k x 16 EEPROMs and 512k x 8 flash memory. An optional A/D module reads 8 SE/4 DI lines with ±10V input range and digitizes to 12 bits with a 9-μsec conversion time.
Acroloop Motion Control Systems (Chaska, MN (612) 448-9800). ***Circle VIP No 107***

Dual-Pentium II motherboard

Built to Intel's NLX motherboard form factor, the 686PCI/64N3C holds dual Pentium IIs using Slot 1 sockets along with as much as 1G byte of DRAM. It also features the Intel BX chipset, which enables 100-MHz SDRAM and memory as well as supports the 100-MHz system bus and the AGP (advanced graphics port) bus. Starting at $595 in OEM qty, the card comes with a CT65554 graphics-accelerator chip and a PCI dual-channel Ultra2SCSI multifunction controller with Ethernet capability. Standard I/O capabilities include two serial ports, USB interface and a parallel port.
Micro Industries Corp (Westerville, OH (800) 722-1842). ***Circle VIP No 108***

Multifunction I/O card

ART D

A bus-mastering PCI card, the $1495 DT3016 combines 32SE/16DI analog inputs with two analog outputs, 16 digital I/O lines and four user-accessible counter/timers. The analog inputs accept full-scale ranges from ±1.25V to ±10V or 0-1.25V to 0-10V; they digitize to 16 bits